SERVICE MANUAL FOR

8066MP

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MiTAC

8066MP N/B Maintenance

Contents

Contents

Contents

1. Hardware Engineering Specification

1.1 Introduction

The MiTAC 8066MP model is designed for Intel Mobile Pentium-M Processor and Celeron-M Processor,Dothan 400 and 533 FSB.

This system is based on PCI architecture and is fully compatible with IBM PC/AT specification, which has standard hardware peripheral interface. The power management complies with Advanced Configuration and Power Interface. It also provides easy configuration through CMOS setup, which is built in system BIOS software and can be pop-up by pressing F2 key at system start up or warm reset. System also provides icon LEDs to display system status, such as Wireless LAN indicator, AC/Battery Power indicator, Battery status indicator, CD-ROM, HDD, NUM LOCK, CAP LOCK, SCROLL LOCK. It also equipped with GIGA LAN, 56K Fax MODEM, 3 USB port, S-Video, line in, SPIDIF, and internal/external microphone function.

The memory subsystem supports DDR2 SDRAM channels (64-bits wide).

The 915GM MCH Host Memory Controller integrates a high performance host interface for Intel Dothan processor, a high performance PCI Express interface, a high performance memory controller, Digital Video port (DVOB & DVOC) interface, and Direct Media Interface (DMI) connecting with Intel ICH6-M.

The Intel ICH6-M integrates three Universal Serial Bus 2.0 Host Controllers Interface (UHCI), the Audio Controller with Azalia interface, the Ethernet includes a 32-bit PCI controller, the IDE Master/Slave controllers, the SATA controller and Direct Media Interface technology.

Intel Graphics enhancements includes DVMT 3.0, Zone Rendering 2.0, Quad pixel pipe rendering engine, Pixel Shader 2.0 and 4x Faster Setup Engine.

The Realtek RTL8110SBL is a highly integrated, cost-effective single-chip Fast Ethernet controller that provides 32-bit performance, PCI bus master capability, and full compliance with IEEE 802.3u 100Base-T specifications and IEEE 802.3x Full Duplex Flow Control. It also supports the Advanced Configuration Power management Interface (ACPI).

The Texas Instruments PCI4510 device is compliant with *PCI Local Bus Specification*. Function 0 provides the independent PC Card socket controller compliant with the latest PC Card Standards. Function 1 of the PCI4510 device is an integrated IEEE 1394a-2000 open host controller interface (OHCI)PHY/link-layer controller (LLC) device that is fully compliant with the PCI Local Bus Specification, the PCI Bus Power Management Interface Specification, IEEE Std 1394-1995, IEEE Std 1394a-2000, and the 1394 Open Host Controller Interface Specification.

The ALC655 is a 16-bit, full duplex AC97 2.3 compatible six channels audio CODEC designed for PC multimedia systems, including host/soft audio and AMR/CNR based designs. The ALC655 incorporates proprietary converter technology to meet performance requirements on PC99/2001 systems.

The W83L950D is a high performance microcontroller on-chip supporting functions optimized for embedded control. These include ROM, RAM, four types of timers, a serial communication interface, optional I²C bus interface, host interface, A/D converter, D/A converter, I/O ports, and other functions needed in control system configurations, so that compact, high performance systems can be implemented easily.

A full set of software drivers and utilities are available to allow advanced operating systems such as Windows ME,

Windows 2000 and Windows XP to take full advantage of the hardware capabilities. Features such as bus mastering IDE, Plug and Play, Advanced Power Management (APM) with application restart, software-controlled power shutdown.

Following chapters will have more detail description for each individual sub-systems and functions.

1.2 System Overview

CPU	Intel: Pentium M 735 Dothan 1.7GHz, 400FSB Intel: Pentium M 770 Dothan 2.13GHz, 533FSB Thermal spec 27W TDP
Core logic	Intel 915GM + ICH6-M chipset
System BIOS	W39V040FAP
Memory	DDR2 RAM: MT8HTF3264HDY-53EB3 (256Mx2) Nanya 533,256MB,NT256T64UH4A0FM-37B
HDD	Fujitsu:MHT2060AT+ , 60GB
ODD	KME: UJ-831BMT-A DVD Dual KME: UJDA760 DVD Combo
Display	15”: Hydis,HT15X34-110 AU: B150XG01
Clock Generator	ICS 954226
TV	Intel 915GM
LAN	RTL8110SBL
PCMCIA + IEEE1394	TI PCI4510
Audio System	AC’97 CODEC: ALC655 Power Amplifier: TI TPA0212
Modem	Askey 1456VQL4A(INT)

1.3 System Hardware Parts

1.3.1 Intel Dothan Processors in Micro-FCBGA package

Intel Dothan Processors with 479 pins Micro-FCBGA package.

It will be manufactured on Intel's advanced 90 nanometer process technology with copper interconnect. It's features include Intel Architecture with Dynamic Execution, On-die primary 32-kB instruction cache and 32-kB write-back data cache, on-die 2-MB second level cache with advanced Transfer Cache Architecture, Data Prefetch Logic, Streaming SIMD Extensions 2 (SSE2), 533-MHz FSB.

The Streaming SIMD Extensions 2 (SSE2) enable break-through levels of performance in multimedia applications including 3-D graphics, video decoding/encoding, and speech recognition.

Use Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock.

Support Enhanced Intel SpeedStep technology, which enables real-time dynamic switching of the voltage and frequency between two performance modes.

1.3.2 Clock Generator

System frequency synthesizer: ICS954226 is a CK410M Compliant clock synthesizer. It provides a single-chip solution for mobile systems built with Intel P4-M processors and Intel mobile chipsets. It is driven with a

14.318MHz crystal and generates CPU outputs up to 400MHz. It provides the tight ppm accuracy required by Serial ATA and PCI-Express.

- Supports tight ppm accuracy clocks for Serial-ATA and SRC
- Supports spread spectrum modulation, 0 to –0.5% down spread
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- Supports undriven differential CPU, SRC pair in PD# for power management

1.3.3 The Mobile Intel 915GM Express Chipset

The Mobile Intel 915GM Express Chipset is a memory controller hub (GMCH) designed for use with the Dothan, Yonah and Intel Celeron M Processor. It supports Intel Graphics Media Accelerator 900 & PCI Express based Graphics.

The 915GM GMCH integrates a system memory DDR/DDR2 controller with two, 64-bit wide interfaces. Only Double Data Rate (DDR/DDR2) memory is supported; the buffers support DDR SSTL_2 and DDR2 SSTL_18 signaling interfaces. The memory controller interface is fully configurable through a set of control registers. It supports a high performance transition interface PCI Express Interface. PCI Express operates at a data rate of 2.5 GB/s. This allows a maximum theoretical bandwidth of 40 GB/s each direction. The 915GM GMCH integrates Direct media interface (DMI) chip-to-chip interconnect between the GMCH and ICH6-M. DMI supports DMI x2 and DMI x4 configuration.

8066MP N/B Maintenance

❖ Processor/FSB Support

- Intel® Dothan processor
- AGTL+ bus driver technology with integrated GTL termination resistors (gated AGTL+ receivers for reduced power)
- Supports 32-bit AGTL+ host bus addressing
- Supports system bus at 533MT/s (533 MHz) and 400MT/s (400 MHz)
- 2X Address, 4X data
- Host bus dynamic bus inversion HDINV support
- 12 deep, in-order queue

❖ Memory System

- Directly supports to two DDR or DDR2 SDRAM channels, 64-bts wide
- Supports SO-DIMMs of the same type (e.g.,all DDR or all DDR2), not mixed
- Maximum of two, double-sided unbuffered SO-DIMMs (4 rows populated)

- Minimum amount of memory supported is 128 MB (16 MB x 16-b x 4 devices x 1 rows = 128 MB) using 256-MB technology
- Maximum amount of memory supported is 2 GB using 1-GB technology
- 256-MB, 512-MB and 1-GB technology using x8 and x16 devices
- Three memory channel organizations are supported for DDR / DDR2
  --- Single channel
  --- dual channel interleaved
  --- dual channel asymmetric
- Supports DDR 333 devices and DDR2 400 /533 devices
  --- Supports on-die termination (ODT) for DDR2
- Supports Fast Chip Select mode
- Supports partial write to memory using Data Mask signal (DM)
- Supports high-density memory package for DDR or DDR2 type devices

❖ **PCI Express Interface**

- One x16 (16 lanes) PCI Express port intended for graphics attach

- Maximum theoretical realized bandwidth on interface of 4 GB/s in each direction simultaneously, for an average of 8 GB/s when x16
- Automatic discovery, negotiation and training of link out of reset
- Supports traditional PCI style traffic (asynchronous snooped, PCI ordering)
- Supports traditional AGP style traffic (asynchronous non-snooped, PCI-X relaxed ordering)
- Supports only 1.5-V AGP electricals
- 32 deep AGP request queue
- Hierarchical PCI-compliant configuration mechanism for downstream devices

❖ **Internal Graphics Controller**

- Intel Dual-Frequency Graphics Technology support
- 3D Graphics Engine

  --- DirectX* 9.0 support

  --- OpenGL* 1.5 and 2.0 support

  --- Zone rendering 2.0 support

8066MP N/B Maintenance

- Analog CRT DAC Interface Support
  --- Supports max DAC frequency up 400 MHz
  --- 24-bit RAMDAC support
  --- DDC2B compliant

- Analog TV-Out Interface Support
  --- Integrated TV-Out device support on display pipes A and B
  --- NTSC/PAL encoder standard formats supported
  --- 480p/720p/1080i/1080p modes supported
  --- Tri-level Sync signal
  --- Multiplexed output interface:
    - Composite video with S-Video
    - S-Video
    - Component Video
  --- Up to 1024 x 768 resolution supported for NTSC/PAL
  --- Macrovision, over scan scaling, and flicker filtering support

- Serial digital video out Port (SDVO) interface Support
  --- Two SDVO port are muxed with a subset of the external graphics interface using PCI Express* Architecture signals
  --- Each SDVO port support display pixel rates up to 200MP/s
    - The two SDVO ports can be combined into a gang mode to support pixel rates up to 400 MP/s

--- Supports a variety display devices such as DVI, TV-Out, LVDS, etc.

--- Supports hot plug and display

--- Supports for Macrovision on SDVO TV-Out devices

--- Supports for HDCP SDVO devices

--- External port adds alpha out

- Digital LVDS Interface Support

--- Integrated dual channel LVDS interface supported on display pipe B only

--- Supports 25-MHz to 112-MHz single/dual channel LVDS LCD interface with support for following format of :

- 1x18 bpp for TFT panels with single channel LVDS
- 2x18 bbp for TFT panels with dual channels LVDS

--- Panel Fitting, Panning, and Center mode supported

--- Spread spectrum clocking (SSC) supported

--- Panel Power Sequencing compliant with SPWG timing specification

--- Integrated PWM interface for LCD backlight inverter control

- Direct Media Interface (DMI)

--- Chip-to-chip interconnect between the GMCH and ICH6-M

--- DMI x2 and DMI x4 configuration supported

--- Bit swapping is supported

--- Lane reversal is not supported

1.3.4 I/O Controller Hub: Intel ICH6-M

❖ **The ICH6 Provides Extensive I/O Support, Functions and Capabilities Include**

- PCI Express Base Specification, Revision 1.0a-compliant
- PCI Local Bus Specification, Revision 2.3-compliant with support for 33 MHz PCI operations(supports up to seven Req/Gnt pairs).
- ACPI Power Management Logic Support
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated Serial ATA host controller with independent DMA operation on two ports and AHCI support
- Integrated IDE controller supports Ultra ATA100/66/33
- USB host interface with support for three USB ports; three UHCI host controllers; one EHCI high-speed USB2.0 Host controller
- Integrated LAN controller
- System Management Bus (SMBus) Specification, Version 2.0 with additional support for I^2C devices
- Supports Audio Codec ’97, Revision 2.3 Specification (a.k.a.,AC ’97 Component Specification, Revision 2.3) which provides a link for Audio and Telephony codecs (up to 7 channels)

- Supports Intel High Definition Audio
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support

1.3.5 CardBus: PCI4510

❖ **The PCI4510 Device Supports the Following Features**

- PC Card Standard 8.0 compliant
- PCI Bus Power Management Interface Specification 1.1 compliant
- Advanced Configuration and Power Interface Specification 2.0 compliant
- PCI Local Bus Specification Revision 2.2 compliant
- PC 98/99 and PC2001 compliant
- Compliant with the PCI Bus Interface Specification for PCI-to-CardBus Bridges
- Fully compliant with provisions of IEEE Std 1394-1995 for a high-performance serial bus and IEEE Std 1394a-2000
- Fully compliant with 1394 Open Host Controller Interface Specification 1.1

8066MP N/B Maintenance

- Compatible with both TPS2211A and TPS2221 PC Card power switches
- 1.8-V core logic and 3.3-V I/O cells with internal voltage regulator to generate 1.8-V core Vcc
- Universal PCI interfaces compatible with 3.3-V and 5-V PCI signaling environments
- Supports PC Card or CardBus with hot insertion and removal
- Supports 132-MBps burst transfers to maximize data throughput on both the PCI bus and the CardBus
- Supports serialized IRQ with PCI interrupts
- Programmable multifunction terminals
- Serial ROM interface for loading subsystem ID and subsystem vendor ID
- ExCA0compatible registers are mapped in memory or I/O space
- Intel 82365SL-DF register compatible
- Supports ring indicate , SUSPEND# , PCI CCLKRUN# protocol , and PCI bus lock (LOCK#)
- Provides VGA/palette memory and I/O , and subtractive decoding options , LED activity terminals
- Fully interoperable with FireWire™ and i.LINK™ implementations of IEEE Std 1394
- Compliant with Intel Mobile Power Guideline 2000

8066MP N/B Maintenance

- Full IEEE Std 1394a-2000 support includes: connection debounce, arbitrated short reset, multispeed concatenation, arbitration acceleration, fly-by concatenation, and port disable/suspend/resume
- Power-down features to conserve energy in battery-powered applications include: automatic device power down during suspend, PCI power management for link-layer and inactive ports powered down, ultra low-power sleep mode
- Two IEEE Std 1394a-2000 fully compliant cable ports at 100M bits/s, 200M bits/s, and 400M bits/s
- Cable power presence monitoring
- Separate cable bias (TPBIAS) for each port
- Physical write posting of up to three outstanding transactions
- PCI burst transfers and deep FIFO to tolerate large host latency
- External cycle timer control for customized synchronization
- Extended resume signaling for compatibility with legacy DV components
- PHY-Link logic performs system initialization and arbitration functions
- PHY-Link encode and decode functions included for data-strobe bit level encoding
- PHY-Link incoming data resynchronized to local clock

8066MP N/B Maintenance

- Low-cost 24.576MHz crystal provides transmit and receive data at 100M bits/s, 200M bits/s, and 400M bits/s
- Node power class information signaling for system power management
- Register bits give software control of contender bit, power class bits, link active control bit, and IEEE Std 1394a-2000 features
- Isochronously receive dual-buffer mode
- Out-of-order pipelining for asynchronous transmit requests
- Register access fail interrupt when the PHY SCLK is not active
- PCI power-management D0, D1, D2, and D3 power states
- Initial bandwidth available and initial channels available registers
- PME# support per 1394 Open Host Controller Interface Specification
- Advanced sub micron, low-power CMOS technology

1.3.6 AC'97 Audio System: ALC655

The ALC655 is a 16-bit, full duplex AC'97 2.3 compatible six channels audio CODEC designed for PC multimedia systems, including host/soft audio and AMR/CNR based designs. The ALC655 incorporates proprietary converter technology to meet performance requirements on PC99/2001 systems. The ALC655 CODEC provides three pairs of stereo outputs with 5-bit volume controls, a mono output, and multiple stereo and mono inputs, along with flexible mixing, gain and mute functions to provide a complete integrated audio solution for PCs. The digital interface circuitry of the ALC655 CODEC operates from a 3.3V power supply for use in notebook and PC applications. The ALC655 integrates 50mW/20ohm headset audio amplifiers at Front-Out and Surr-Out, built-in 14.318M→24.576MHz PLL and PCBEEP generator, those can save BOM costs. The ALC655 also supports the S/PDIF input and output function, which can offer easy connection of PCs to consumer electronic produces, such as AC3 decoder/speaker and mini disk devices. ALC655 supports host/soft audio from Intel ICHx chipsets as well as audio controller based VIA/SIS/ALI/AMD/nVIDIA/ATI chipset. Bundled Windows series drivers (WinXP/ME/2000/98/NT), EAX/Direct Sound 3D/I3DL2/A3D compatible sound effect utilities (supporting Karaoke, 26-kind of environment sound emulation, 10-band equalizer), HRTF 3D positional audio and Sensaura™ 3D (optional) provide an excellent entertainment package and game experience for PC users. Besides, ALC655 includes Realtek's impedance sensing techniques that makes device load on outputs and inputs can be detected.

❖ Features

- Meets performance requirements for audio on PC99/2001 systems
- Meets Microsoft WHQL/WLP 2.0 audio requirements
- 16-bit Stereo full-duplex CODEC with 48KHz sampling rate

8066MP N/B Maintenance

- Compliant with AC'97 2.3 specifications
  ---Front-Out, Surround-Out, MIC-In and LINE-In Jack Sensing
  ---14.318MHz→24.576MHz PLL to save crystal
  ---12.288MHz BITCLK input can be consumed
  ---Integrated PCBEEP generator to save buzzer
  ---Interrupt capability
- Three analog line-level stereo inputs with 5-bit volume control: LINE_IN, CD, AUX
- High quality differential CD input
- Two analog line-level mono input: PCBEEP, PHONE-IN
- Two software selectable MIC inputs
- LINE Input shared with surround output: MIC input shared with Center and LFE output
- Both Front-out and Surround-Out built-in 50mW/20ohm amplifier
- External Amplifier Power Down (EAPD)
- Power management and enhanced power saving features
- Stereo MIC record for AEC/BF application
- Supports Power Off CD function

- Adjustable VREFOUT control
- Supports double sampling rate (96KHz) of DVD audio playback
- Support 48KHz of S/PDIF output is compliant with AC'97 rev2.3 specification
- Support 32K/44.1K/48KHz of S/PDIF input
- Power support: Digital: 3.3V; Analog: 3.3V/5V
- Standard 48-Pin LQFP Package
- EAX™ 1.0 & 2.0 compatible
- Direct Sound 3D™ compatible
- HRTF 3D Positional Audio
- Sensaura™ 3D Enhancement (optional)
- 10 Bands of Software Equalizer
- Voice Cancellation and Key Shifting in Kara OK mode
- AVRack Media Player
- Configuration Panel to improve Experience of User

1.3.7 Modem: Askey 1456VQL4A(INT) Data/Fax Modem

Features

- ITU-T V.90/V.92 data rates 28000 bits/s-56000 bits/s
- High compression throughput due to parallel access directly to the host PC
- ITU-T V.34 extended rates: 33600 bits/s-2400 bits/s V.32terbo, V.32bis, and fallbacks.
- ITU-T V.42 error correction (LAPM and MNP)
- ITU-T V.42bis V.44 and MNP Class 5 data compression
- Supports fax ITU-T V.34, V.17, V.29, V.27ter, and V.21 Ch 2
- ITU-T V.253 Class 1 FAX
- Support Application for Windows 98, Windows 98SE, Windows NT 4.0, Windows 2000, Windows XP
- AC97/MC'97 2.2 compliant

1.3.8 System Flash Memory (BIOS)

❖ Features

- Single 3.3-volt operations:

  ---3.3V Read

  ---3.3V Erase

  ---3.3V Program

- Fast Program operation:

  ---Byte-by-Byte programming: 35uS (typ.)

- Fast Erase operation:

  ---Chip erase 100mS (max.)

  ---Sector erase 25mS (max.)

  ---Page erase 25mS (max.)

- Fast Read access time: Tkq 11nS

- Endurance: 10K cycles (typ.)

- 8 Even sectors with 64K bytes each, which is composed of 16 flexible pages with 4K bytes

- Any individual sector or page can be erased

- Hardware protection:

  ---Optional 16K byte or 64K byte Top Boot Block with lockout protection

  ---#TBL & #WP support the whole chip hardware protection

  ---Flexible 4K page size can be used as Parameter Blocks

  ---Low power consumption. Active current: 40mA (typ. For FWH mode)

  ---Automatic program and erase timing with internal Vpp generation

  ---End of program or erase detection: Toggle bit; Data polling

  ---Latched address and data

1.3.9 Memory System

❖ **256MB, 512MB, 1GB (x64) 200-Pin DDR2 SDRAM SODIMMs**

- JEDEC-standard 200-pin, small-outline, dual in-line memory module (SODIMM)
- VDD=+1.8V±0.1V, VDDQ=+1.8V±0.1V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS,DQS#) option
- Four-bit prefetch architecture
- Differential clock input (CK,CK#)

- Command entered on each rising CK edge
- DQS edge-aligned with data for Reads
- DQS center-aligned with data for Writes
- Duplicate output strobe (RDQS) option for x8 configuration
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data
- Programmable CAS Latency (CL) : 2,3,4 and 5
- Posted CAS additive latency (AL) : 0,1,2,3 and 4
- Write latency = Read latency – 1^{t}CK
- Programmable burst lengths : 4 or 8
- Read burst interrupt supported by another READ
- Write burst interrupt supported by another WRITE
- Adjustable data – output drive strength

- Concurrent auto precharge option is supported
- Auto Refresh (CBS) and Self Refresh Mode
- 64ms, 8,192-cycle refresh
- Off-chip drive (OCD) impedance calibration
- On-die termination (ODT)

1.3.10 LAN – Integrated Gigabit Ethernet Controller

The Realtek RTL8110SBL (128 LQFP) Gigabit Ethernet controllers combine a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, 32-bit PCI bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, they offer high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The devices support the PCI v2.3 bus interface for host communications with power management and are compliant with the IEEE 802.3 specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. They also support an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space.

They support the Advanced Configuration Power management Interface (ACPI) – power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM) – to achieve the most efficient power management possible. PCI Message Signaled Interrupt (MSI) is also supported.

In addition to the ACPI feature, the RTL8110SBL support remote wake-up (including AMD Magic Packet, Re-LinkOk, and Microsoft Wake-up frame) in both ACPI and APM (Advanced Power Management) environments.

The RTL8110SBL is fully compliant with Microsoft NDIS5 (IP, TCP, UDP) Checksum and Segmentation Task-offload features, and supports IEEE 802 IP Layer 2 priority encoding and 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server. Also, the devices boost their PCI performance by supporting PCI Memory Read Line & Memory Read Multiple when transmitting, and Memory Write and Invalidate when receiving. To better qualify for server use, the RTL8110SBL support the PCI Dual Address Cycle (DAC) command when the assigned buffers reside at a physical memory address higher than 4 Gigabytes.

❖ Features

- Integrated 10/100/1000 transceiver
- Auto-Negotiation with Next Page capability
- Supports PCI rev 2.3, 32-bit, 33/66MHz
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction

8066MP N/B Maintenance

- Wake-on-LAN and remote wake-up support
- Microsoft NDIS5 Checksum Offload (IP, TCP, UDP) and large send offload support
- Supports Full Duplex flow control (IEEE 802.3x)
- Fully compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab
- Support IEEE 802.1P Layer 2 Priority Encoding
- Support IEEE 802.1Q VLAN tagging
- Serial EEPROM
- 3.3V signaling, 5V PCI I/O tolerant
- Transmit/Receive FIFO (8K/64K) support
- Supports power down/link down power saving
- Supports PCI Message Signaled Interrupt (MSI)
- 128-pin LQFP package

1.3.11 Keyboard System: Winbond W83L950D

The Winbond Keyboard controller architecture consists of a Turbo 51 core controller surrounded by various registers, nine general purpose I/O port, 2k+256 bytes of RAM, four timer/counters, dual serial ports, 40K MTP-ROM that is divided into four banks, two SMBus interface for master and slave, Support 4 PWM channels, 2 D-A and 8 A-D converters.

❖ Features

- 8051 uC based
- Keyboard Controller Embedded Controller
- Supply embedded programmable flash memory (internal ROM size: 40KB) and RAM size is 2 KB.
- Support 4 Timer (8 bit) signal with 3 prescalers.
- Support 2 PWM channels, 2 D-A and 8 A-D converters.
- Reduce Firmware burden by Hardware PS/2 decoding
- Support 72 useful GPIOs totally
- Support Flash utility for on board re-flash
- Support ACPI

- Hardware fast Gate A20 with software programmable

1.3.12 Hard Disk Drive

8066MP can support SATA or PATA HDD by equipped different HDD transition board.

SATA HDD: The SATA function in the ICH6 has dual modes of operation to support different operating system conditions. In the case of Native IDE enabled operating systems, the ICH6 has separate PCI functions for serial and parallel ATA ("enhanced mode"). To support legacy operating systems, there is only one PCI function for both the serial and parallel ATA ports if functionality from both SATA and PATA devices is desired ("combined mode"). SATA interface transfer rates are independent of UDMA mode settings. SATA interface transfer rates will operate at the bus's maximum speed, regardless of the UDMA mode reported by the SATA device or the system BIOS.

❖ **Features**

- Up-to 150MB/sec bus speed (Serial ATA Generation 1)
- Compliant with Serial ATA 1.0a Specification and Serial ATA 2 Extensions 1.0.
- Supports 48bit-LBA addressing
- Supports Native DMA Queued command (First party DMA queued)
- Also supports Legacy DMA Queued command

- Supports Staggered Spin-Up function
- Supports Hot-Plug features
- Supports Serial ATA power management (Host initiated Partial/Slumber)

IDE HDD: The ICH6 IDE controller features one set of interface signals that can be enabled, tri-stated or driven low.

❖ **The IDE Interfaces of the ICH6 can Support Several Types of Data Transfers:**

- Programmed I/O (PIO): processor is in control of the data transfer.
- 8237 style DMA: DMA protocol that resembles the DMA on the ISA bus, although it does not use the 8237 in the ICH6. This protocol off loads the processor from moving data. This allows higher transfer rate of up to 16MB/s.
- Ultra ATA/33/66/100: DMA protocol that redefines signals on the IDE cable to allow both host and target throttling of data and transfer rates of up to 33/66/100 MB/s.

1.4 Other Functions

1.4.1 Hot Key Function

Keys Combination	Feature	Meaning
Fn + F1	Wireless LAN ON/OFF	Wireless LAN turn on and turn off
Fn + F2	Reserve	
Fn + F3	Volume Down	Decrease speaker volume
Fn + F4	Volume Up	Increase speaker volume
Fn + F5	LCD/external CRT switching	Rotate display mode in LCD only, CRT only, and simultaneously display.
Fn + F6	Brightness down	Decreases the LCD brightness
Fn + F7	Brightness up	Increases the LCD brightness
Fn + F10	Speaker ON/OFF	Toggle speaker on/off
Fn + F11	Panel ON/OFF	Toggle Panel on/off
Fn + F12	Suspend to RAM	Force the computer into Suspend to DRAM mode depending on BIOS Setup.

1.4.2 Power On/Off/Suspend/Resume Button

1.4.2.1 APM Mode

At APM mode, power button is on/off system power.

1.4.2.2 ACPI Mode

At ACPI mode, windows power management control panel set power button behavior.

You could set “standby” , “power off” or “hibernate”(must enable hibernate function in power management) to power button function. Continue pushing power button over 4 seconds will force system off at ACPI mode.

1.4.3 Cover Switch

System automatically provides power saving by monitoring Cover Switch. It will save battery power and prolong the usage time when user closes the notebook cover.

At ACPI mode there are four functions to be chosen at windows power management control panel.

1. None
2. Standby

3. Off

4. Hibernate (must enable hibernate function in power management)

1.4.4 LED Indicators

System has eight status LED indicators to display system activity, which include three at the lower side of Panel cover, five in the front-left edge of the notebook.

1.4.4.1 Three LED Indicators on LCD Housing and above Keyboard:

From left to right that indicates WLAN, Power, Battery Status.

AC / Battery Power

This LED lights green when the notebook was powered by AC or battery power line, Flashes (on 1 second, off 1 second) when entered suspend to RAM state . The LED is off when the notebook is in power off state.

Battery Charge Status (Operate at both system on and off)

With battery operation, this LED stays off. When the battery charge drops to 10% of capacity, the LED lights red, flashes per 1 second and beeps per 2 second. When AC is connected, this indicator glows green if the battery pack is fully charged or orange (amber) if the battery is being charged.

Wireless LAN

This LED light green when the wireless LAN is enabled.

1.4.4.2 Five LED Indicators in the Front Side of the Notebook:

From left to right that indicates CD-ROM, HARD DISK, NUM LOCK, CAPS LOCK and SCROLL LOCK.

1.4.5 Battery Status

1.4.5.1 Battery Warning

System also provides Battery capacity monitoring and gives user a warning so that users have chance to save his data before battery dead. Also, this function protects system from mal-function while battery capacity is low.

Battery Warning: Capacity below 10%, Battery Capacity LED flashes per second, system beeps per 2 seconds.

System will suspend to HDD after 2 Minutes to protect users data.

1.4.5.2 Battery Low State

After Battery Warning State, and battery capacity is below 5%, system will generate beep sound for twice per second.

1.4.5.3 Battery Dead State

When the battery voltage level reaches 8.56 volts, system will shut down automatically in order to extend the battery packs' life.

1.4.6 Fan Power On/Off Management

FAN is controlled by W83L950D embedded controller-using ADT7460 to sense CPU temperature and PWM control fan speed. Fan speed is depended on CPU temperature. Higher CPU temperature will get faster Fan Speed.

1.4.7 CMOS Battery

CR2032 3V 220mAh lithium battery.When AC in or system main battery inside, CMOS battery will consume no power.AC or main battery not exists, CMOS battery life at less (220mAh/5.8uA) 4 years.

1.4.8 I/O Port

- One Power Supply Jack
- One External CRT Connector For CRT Display
- Supports three USB port for all USB devices
- One MODEM RJ-11 phone jack for PSTN line
- One RJ-45 for LAN
- One IEEE1394 port
- One S/PDIF Jack
- One Line-In Jack
- One Microphone Input Jack
- One S-Video (PAL/NTSC) connector

1.4.9 Battery Current Limit and Learning

Implanted H/W current limit and battery learning circuit to enhance protection of battery.

1.5 Power Management

The 8066MP system has built in several power saving modes to prolong the battery usage for mobile purpose. User can enable and configure different degrees of power management modes via ROM CMOS setup (booting by pressing F2 key). Following are the descriptions of the power management modes supported.

1.5.1 System Management Mode

1.5.1.1 Full On Mode

In this mode, each devices is running with the maximal speed. CPU clock is up to its maximum.

1.5.1.2 Doze Mode

In this mode, CPU will be toggling between on & stop grant mode either. The technology is clock throttling. This can save battery power without loosing much computing capability.

The CPU power consumption and temperature is lower in this mode.

1.5.1.3 Standby Mode

For more power saving, it turns off the peripheral components. In this mode, the following is the status of each device:

- CPU: Stop grant
- LCD: Backlight off
- HDD: Spin down

1.5.1.4 Suspend to DRAM and HDD

The most chipset of the system is entering power down mode for more power saving. In this mode, the following is the status of each device:

- **Suspend to DRAM**
  - CPU: off
  - Intel 915GM : Partial off
  - VGA: Suspend
  - PCMCIA: Suspend
  - Audio: off
  - SDRAM: Self Refresh

- **Suspend to HDD**
  - All devices are stopped clock and power-down
  - System status is saved in HDD
  - All system status will be restored when powered on again

1.5.2 Other Power Management Functions

HDD & Video access: System has the ability to monitor video and hard disk activity. User can enable monitoring function for video and/or hard disk individually. When there is no video and/or hard disk activity, system will enter next PMU state depending on the application. When the VGA activity monitoring is enabled, the performance of the system will have some impact

1.6 Appendix 1: Intel ICH6-M GPIO Definitions -1

Pin name	Current Define		Power plane
GPIO0	SDIRQ	I	MAIN
GPIO1	MINIPCI_ACT#	I	MAIN
GPIO2	PCI_INTE#	I	MAIN
GPIO3	PCI_INTF#	I	MAIN
GPIO4	PCI_INTG#	I	MAIN
GPIO5	PCI_INTH#	I	MAIN
GPIO7	SCI#	I	MAIN
GPIO8	EXTSMI#	I	RESUME
GPIO9	X	I	RESUME
GPIO10	X	I	RESUME
GPIO11	SMBALERT#	I	RESUME
GPIO12	KBD_US/JP#	I	MAIN
GPIO13	WAKE_UP#	I	RESUME
GPIO14	X	I	RESUME
GPIO15	X	I	RESUME
GPIO16	X	O	MAIN
GPIO17	X	O	MAIN
GPIO19	X	O	MAIN

1.6 Appendix 1: Intel ICH6-M GPIO Definitions -2

Continue to previous page

Pin name	Current Define		Power plane
GPIO21	X	O	MAIN
GPIO23	WIRELESS_PD#	O	MAIN
GPIO24	SPK_OFF	I/O	RESUME
GPIO25		I/O	RESUME
GPIO26	PANEL_ID0	I	MAIN
GPIO27	X	I/O	RESUME
GPIO28	X	I/O	RESUME
GPIO29	PANEL_ID1	I	MAIN
GPIO30	PANEL_ID2	I	MAIN
GPIO31	PANEL_ID3	I	MAIN
GPIO33	MB_ID0	I/O	MAIN
GPIO34	MB_ID1	I/O	MAIN
GPIO40	MXM_DETECT#	I	MAIN
GPIO41	CRT_IN#	I	MAIN
GPIO48	X	O	MAIN
GPIO49	HPWRGD	OD O	MAIN

1.7 Appendix 2: W83L950D KBC Pins Definitions -1

Port	pin	Function	Implement
P0	0-7	Scan matrix	KO[0..7]
P1	0-7		KO[8..15]
P3	0-7		KI[0..7]
P2	0	LPC enable	H8_THRM#
	1	GPIO x1	H8_WAKE_UP#
	2	SMBUS1 or UART	BATT_G#
	3		BATT_R#
	4	GPIO x4	EXTSMI#
	5		CAP#
	6		NUM#
	7		SCROLL#
P4	0	Xcin/cout or PWM 2,3	H8_ENABKL
	1		CHARGING
	2	GPIO x2 (INT1)	LEARING
	3		H8_SUSB
	4	KBRST	H8_HRCIN#
	5	A20	A20GATE
	6	GPIO x2	H8_SCI
	7		H8_PWRON

1.7 Appendix 2: W83L950D KBC Pins Definitions -2

Continue to previous page

Port	pin	Function	Implement
P5	0	GPIO x1	SW_VDD3
	1	GPIO x3 (INT20,30,40)	H8_LIDSW#
	2		BATT_DEAD#
	3		H8_ADEN#
	4	GPIO x2	BATT_LED#
	5		KBC_PWRON_VDD3S
	6	D/A, PWM 2,3	BLADJ
	7		H8_I_CTR
P6	0	A/D (INT5-12)	PWRBTN#
	1		KBC_RI#
	2		AC_ POWER#
	3		BATT_V
	4		BATT_T
	5		H8_I_LIMIT
	6		H8_PROCHOT#
	7		+BC_CPUCORE

1.7 Appendix 2: W83L950D KBC Pins Definitions -3

Continue to previous page

Port	pin	Function	Implement
P7	0	PS/2 port x3	T_DATA
	1		H8_RSMRST
	2		ICH_PWRBTN
	3		T_CLK
	4		H8_PWRON_SUSB#
	5		SUSC#
	6	SMBUS	BAT_DATA
	7		BAT_CLK
P8	0	LPC interface	PCICLK_KBC
	1		SERIRQ
	2		LAD3
	3		LAD2
	4		LAD1
	5		LAD0
	6		KBC_PCIRST#
	7		LFRAME#

1.8 Appendix 3: 8066MP Product Specifications -1

8066MP Preliminary Specifications R0.6	
Model	**8066MP**
CPU	Intel Pentium-M Processor Dothan 400 and 533 FSB -Thermal spec 35W TDP
Chip Set	Intel 915GM+ICH6M
L2 Cache	2MB for Dothan
System BIOS	512KB Flash EPROM - include System BIOS, VGA BIOS – Plug &Play capability -ACPI
Memory	0MB DDRII 400/533 SDRAM memory on board - 2 memory DIMM slots for memory expansion - 200pin DDRII 400/533 SDRAM SO-DIMM Memory Module Support up to 2048MB - 1.25-inch height memory module supported
Video Controller	SMA
Optical drive	Combo / DVD+RW, DVD-RW, DVD-Dual (12.7mm) Detected as 2nd Master (by ODD F/W)
FDD	External USB I/F Option
HDD	Support 2.5" 30GB / 40GB / 60GB / 80GB/100GB/120GB HDD(9.5mm) 4200rpm or 5400rpm Ultra DMA(PATA) 100
Display	14.1"/15" XGA TFT -Resolution: 1024x768

1.8 Appendix 3: 8066MP Product Specifications -2

Continue to previous page

Keyboard	European keyboard layout - 19mm key pitch / 3mm stroke - Hot key spec: Fn+F1 : WirelessLAN ON/OFF , Fn+F3/F4 : Volume down/up, Fn+F5 : LCD/CRT output change Fn+F6/F7: Brightness up/down, Fn+F11: Display ON/OFF, Fn+F12: Standby
Pointing Device	TouchPad (No scroll button)
PC Card Slot	TypeII x 1 -PCMCIA Standard Rev.2.1 , CardBus support , w/o ZV port
Audio System	Built-in Sound system - AC97 1/F (5.1 CH support) - AC-3 support - Built-in stereo speaker, Built-in microphone - Sound Volume control by Hot-Key (Fn + F3 : Volume down, Fn + F4 : Volume up)
I/O Port	USB(2.0) x 3 Mic-in x 1(Mono);Line-in x 1 SPDIF x 1 (AC97) S-Video (PAL/NTSC) x 1 RJ-45 LAN Jack x 1 (with cap) RJ-11Modem Jack x 1 (with cap) IEEE 1394 x 1 VGA port x 1 DC-in x 1

1.8 Appendix 3: 8066MP Product Specifications -3

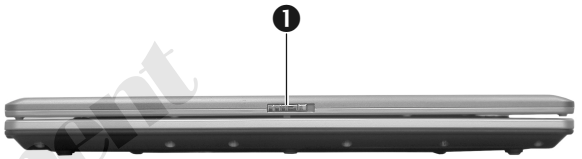
Continue to previous page

Communication	56Kbps(V.90) Fax Modem(MDC(Azalia I/F)) and 10/100/1000 Base-TX LAN Wireless LAN (Mini PCI Interface IEEE802.11b, g)
Battery	Li-ion Battery 2400mAh(6-cell) - Battery Life: 3 hrs(256+256MB Memory, Dothan 1.7GHz CPU, Backlight: Mid.) Power-ON charge available -RTC backup battery(Lithium) Standard
Indicator	5 LEDs at parm rest: ODD/HDD/Number Lock/Caps Lock/Scroll Lock 3 LEDs above keybaord: WLAN/Power/Battery status 3 LEDs on LCD housing: WLAN/Power/Battery status
Quick Keys	3 Quick keys: Internet/e-mail/battery low alarm on-off
Power Supply	65W(P) Universal AC Adapter(100-240V)
Safety Lock	Kensington Lock x 1
Dimension	W277 x D329 x H26~33.3mm
WEIGHT	2.7kg (P)
OS	Windows XP Pro (With SP2)
Windows Logo	Support PC2001 Specification - Need to get the Log files for WindowsXP Pro, WHQL Certified
EMI/Safety/ Regulation	EMI:CE/TUV/CB RF:R&TTE PTT:CE

2. System View and Disassembly

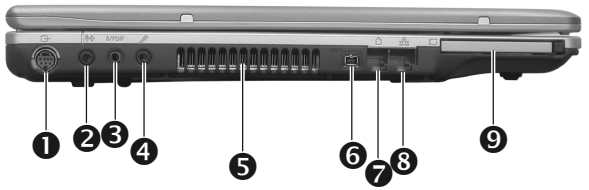
2.1 System View

2.1.1 Front View



❶ Top Cover Latch

2.1.2 Left-side View



❶ S-Video Port
❷ Line In Connector
❸ S/PDIF Connector
❹ MIC In Connector
❺ Ventilation Openings
❻ IEEE1394 Connector
❼ RJ-11 Connector
❽ RJ-45 Connector
❾ PCMCIA Card Socket

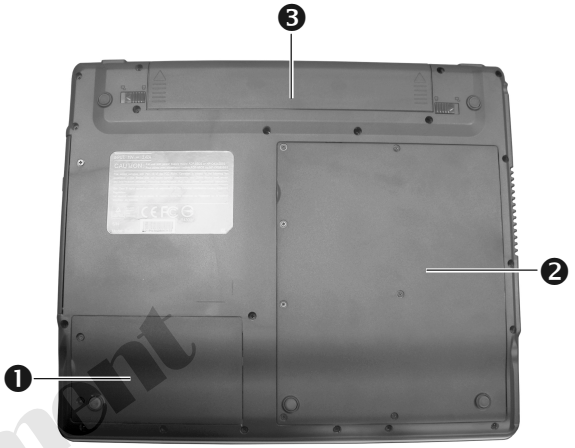
2.1.3 Right-side View

❶ CD/DVD-ROM Drive
❷ USB Port *1
❸ Power Connector

2.1.4 Rear View

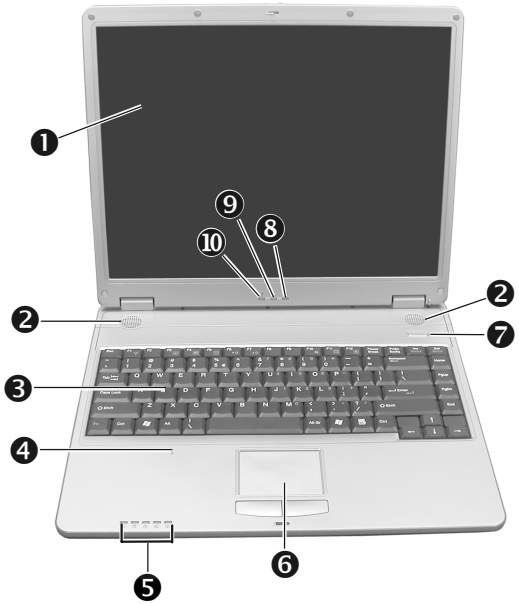
❶ Lock
❷ USB Ports *2
❸ VGA Port

2.1.5 Bottom View



❶ Hard Disk Drive
❷ CPU
❸ Battery Park

2.1.6 Top-open View

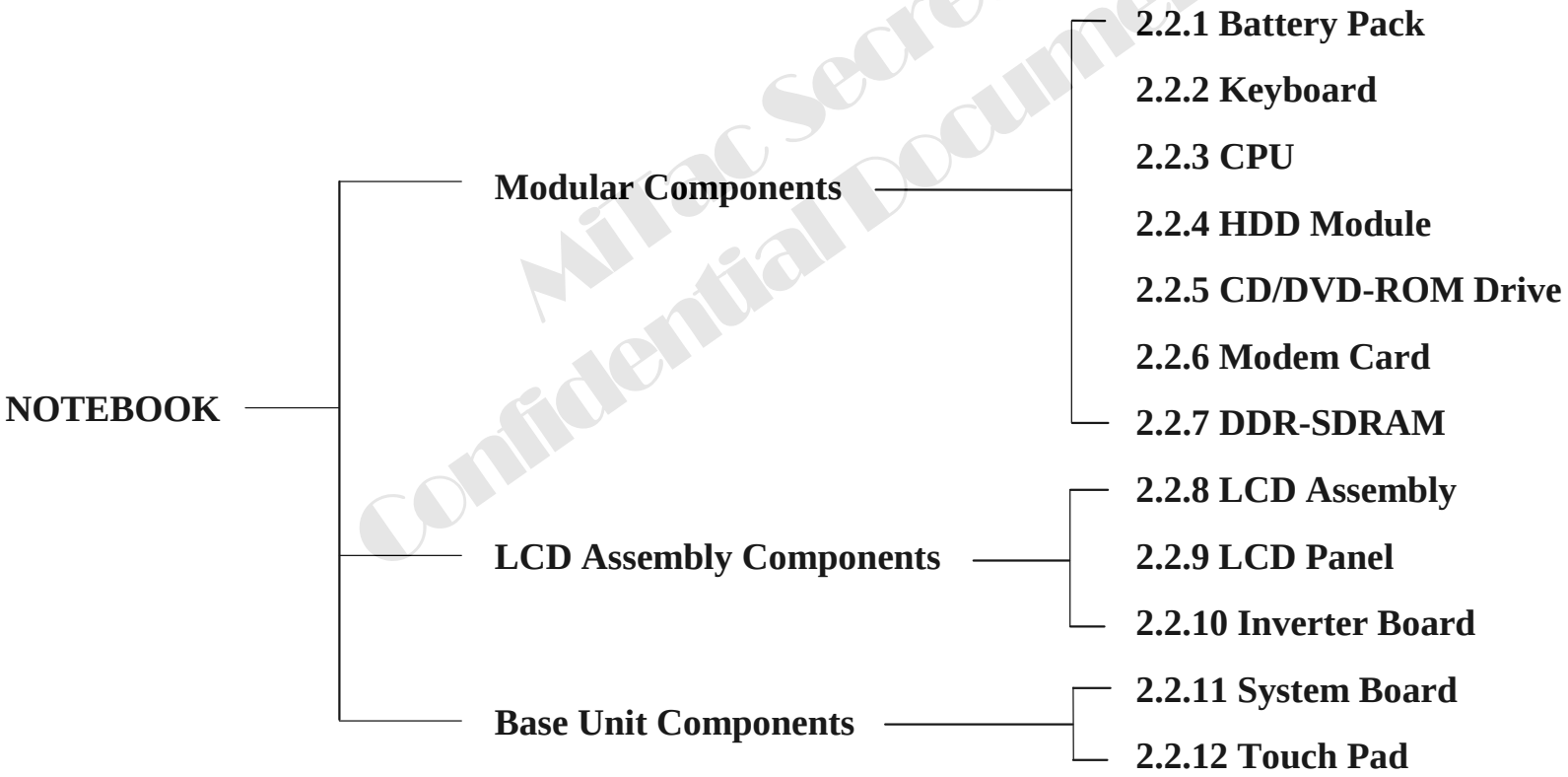


❶ LCD Screen
❷ Stereo Speaker Set
❸ Keyboard
❹ Internal MIC In
❺ Device LED Indicators
❻ Touch Pad
❼ Power Button
❽ Battery Indicator
❾ Power Indicator
❿ Wireless Indicator

2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations.Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Slide the two release lever outwards to the "unlock" ( ) position (❶), while take the battery pack out of the compartment (❷). (Figure 2-1)

Figure 2-1 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the "lock" ( ) position.

2.2.2 Keyboard

Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Push the keyboard cover to loose the locks from the battery compartment. (Figure 2-2)
3. Lift the keyboard cover up. (Figure 2-3)

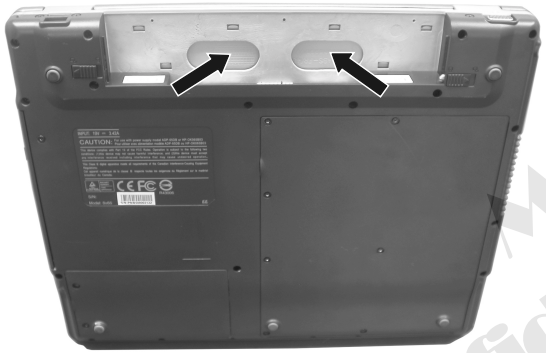


Figure 2-2 Push the keyboard cover

Figure 2-3 Lift the keyboard cover

4. Slightly lift up the keyboard. (Figure 2-4)
5. Disconnect the cable from the system board, then separate the keyboard. (Figure 2-5)

Figure 2-4 Lift the keyboard

Figure 2-5 Disconnect the cable

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the keyboard cover.
3. Replace the battery pack. (Refer to section 2.2.1 Reassembly)

2.2.3 CPU

Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove the seven screws fastening the CPU cover. (Figure 2-6)
3. Remove the four spring screws that secure the heatsink upon the CPU and disconnect the fan's power cord from system board. (Figure 2-7)

Figure 2-6 Remove the seven screws

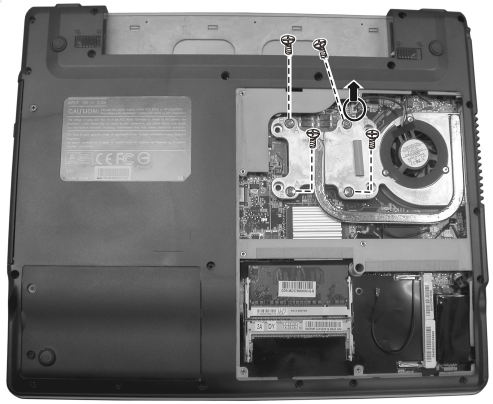


Figure 2-7 Free the heatsink

4. To remove the existing CPU, loosen the screw by a flat screwdriver,upraise the CPU socket to unlock the CPU. (Figure 2-8)

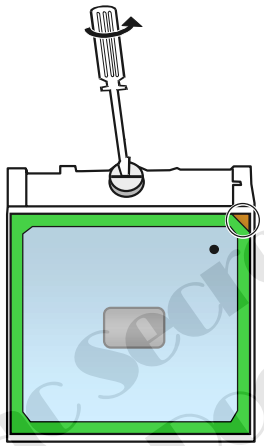


Figure 2-8 Remove the CPU

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Tighten the screw by a flat screwdriver to locking the CPU.
2. Connect the fan's power cord to the system board, fit the heatsink upon the CPU and secure with four spring screws.
3. Replace the CPU cover and secure with seven screws.
4. Replace the battery pack. (Refer to section 2.2.1 Reassembly)

2.2.4 HDD Module

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove the two screws fastening the HDD compartment cover. (Figure 2-9)
3. Remove the one screw and slide the HDD module out of the compartment. (Figure 2-10)

Figure 2-9 Remove the HDD compartment cover

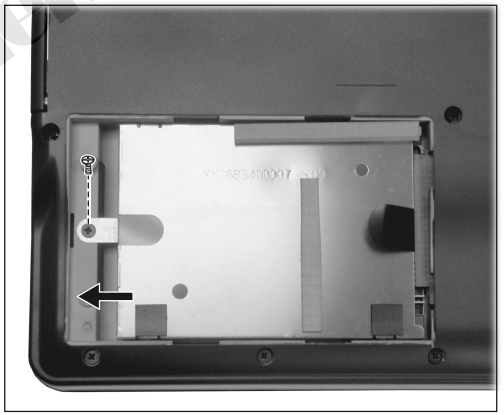


Figure 2-10 Remove HDD module

4. Remove the four screws to separate the hard disk drive from the bracket, remove the hard disk drive. (Figure 2-11)

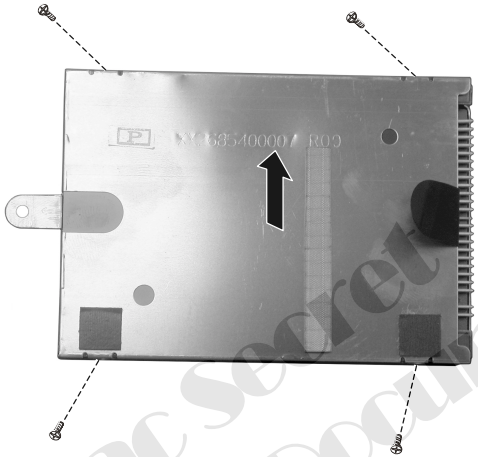


Figure 2-11 Remove hard disk drive

Reassembly

1. Attach the bracket to hard disk drive and secure with four screws.
2. Slide the HDD module into the compartment and secure with one screw.
3. Place the HDD compartment cover and secure with two screws.
4. Replace the battery pack. (Refer to section 2.2.1 Reassembly)

2.2.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove the one screw fastening the CD/DVD-ROM drive. (Figure 2-12)
3. Insert a small rod, such as a straightened paper clip, into CD/DVD-ROM drive's manual eject hole (❶) and push firmly to release the tray. Then gently pull out the CD/DVD-ROM drive by holding the tray that pops out (❷). (Figure 2-12)

Figure 2-12 Remove the CD/DVD-ROM drive

Reassembly

1. Push the CD/DVD-ROM drive into the compartment and secure with one screw.
2. Replace the battery pack. (Refer to section 2.2.1 Reassembly)

2.2.6 Modem Card

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove the seven screws fastening the CPU cover. (Refer to step 2 of section 2.2.3 Disassembly)
3. Remove the two screws fastening the modem card. (Figure 2-13)
4. Lift up the modem card and disconnect the cord. (Figure 2-14)

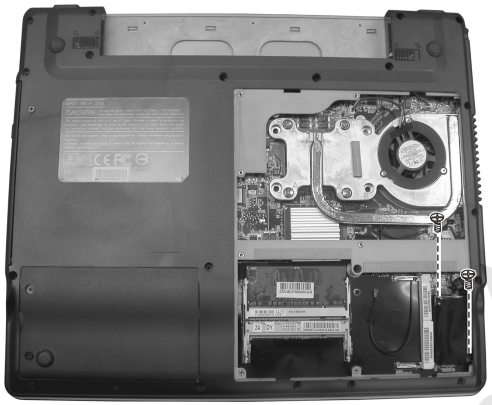


Figure 2-13 Remove the two screws

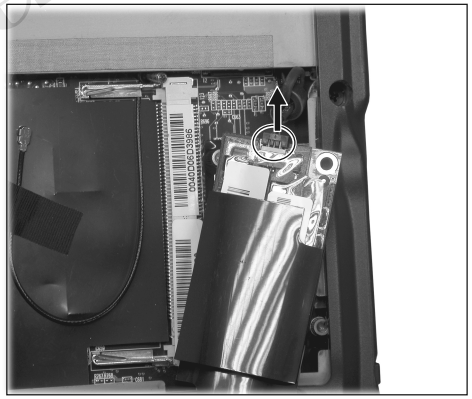


Figure 2-14 Disconnect the cord

Reassembly

1. Reconnect the cord and fit the modem card.
2. Fasten the modem card by two screws.
3. Replace the CPU cover and secure with seven screws. (Refer to step 3 of section 2.2.3 Reassembly)
4. Replace the battery pack. (Refer to section 2.2.1 Reassembly)

2.2.7 DDR-SDRAM

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (See section 2.2.1 Disassembly)
2. Remove the seven screws fastening the CPU cover. (Refer to step 2 of section 2.2.3 Disassembly)

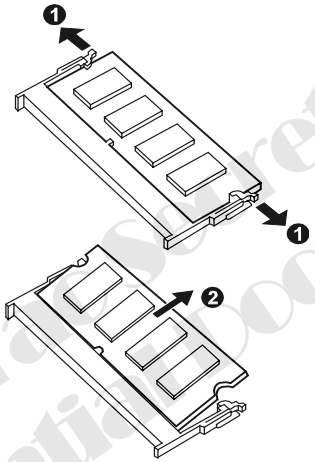


Figure 2-15 Remove the SO-DIMM

3. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-15)

Reassembly

1. To install the DDR, match the DDR's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR into position.
2. Replace the CPU cover and secure with seven screws. (Refer to step 3 of section 2.2.3 Reassembly)
3. Replace the battery pack. (See section 2.2.1 Reassembly)

2.2.8 LCD ASSY

Disassembly

1. Remove the battery pack and keyboard. (See sections 2.2.1 and 2.2.2 Disassembly)
2. Separate the antenna from the system board. (Figure 2-16)
3. Remove the two hinge covers, then carefully pull the antenna wires out. (Figure 2-17)

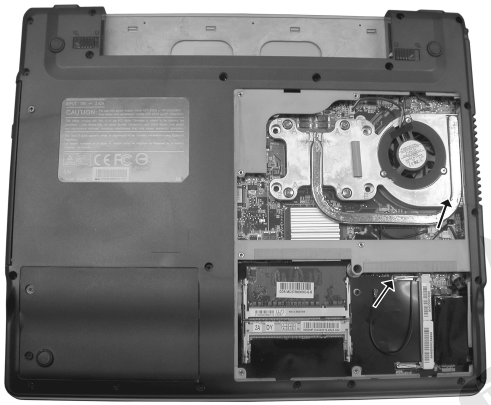


Figure 2-16 Separate the antenna

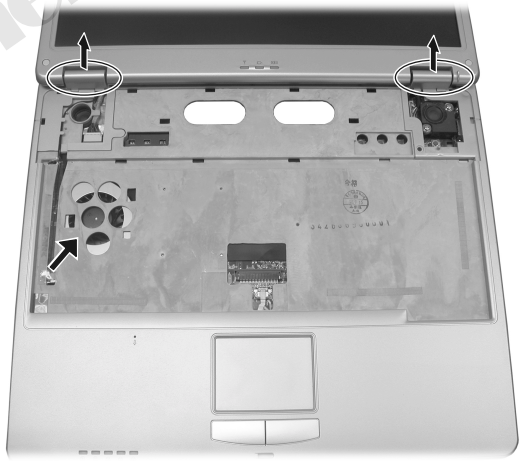


Figure 2-17 Remove the two hinge covers

4. Disconnect the two cables from the system board. (Figure 2-18)
5. Remove the four screws, then free the LCD assembly. (Figure 2-19)

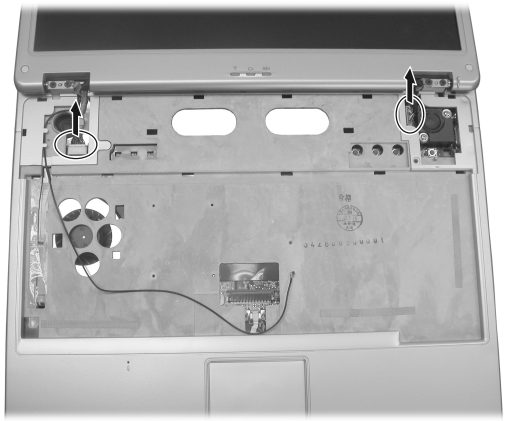


Figure 2-18 Disconnect the two cables

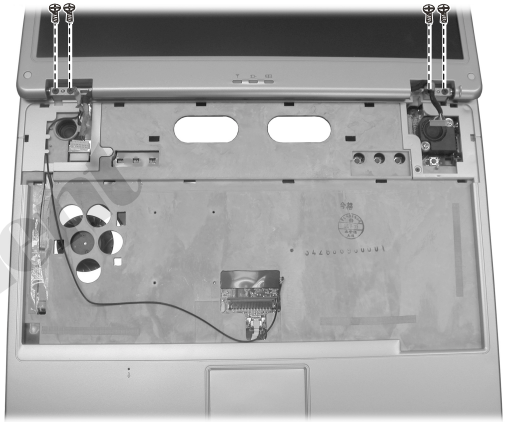


Figure 2-19 Free the LCD assembly

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws.
2. Replace the antenna wires back into Mini PCI compartment.
3. Reconnect the two cables to the system board.
4. Replace the keyboard and battery pack. (Refer to sections 2.2.2 and 2.2.1 Reassembly)

2.2.9 LCD Panel

Disassembly

1. Remove the battery, keyboard and LCD assembly. (Refer to section 2.2.1, 2.2.2 and 2.2.8 Disassembly)
2. Remove the two rubber pads and two screws on the corners of the panel. (Figure 2-20)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
4. Remove the eight screws and disconnect the cable. (Figure 2-21)

Figure 2-20 Remove LCD cover

Figure 2-21 Remove the eight screws and disconnect the cable

5. Remove the four screws that secure the LCD brackets. (Figure 2-22)
6. Disconnect the cable to free the LCD panel. (Figure 2-23)

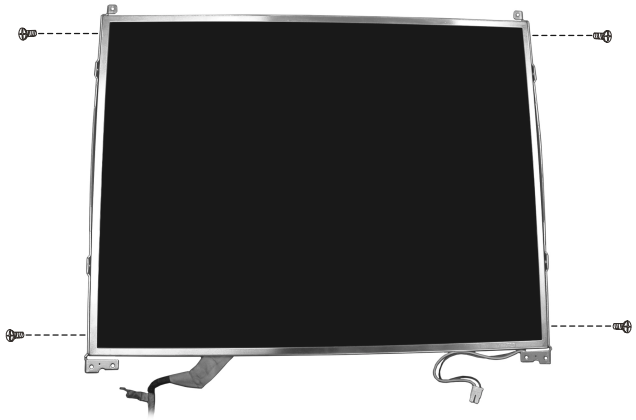


Figure 2-22 Remove the four screws

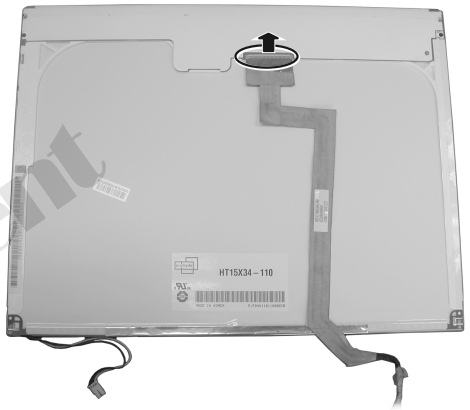


Figure 2-23 Free the LCD panel

Reassembly

1. Replace the cable to the LCD panel.
2. Attach the LCD panel's brackets back to LCD panel and secure with four screws.
3. Replace the LCD panel into LCD housing and secure with eight screws.
4. Reconnect one cable to inverter board.
5. Fit the LCD cover and secure with two screws and rubber pads.
6. Replace the LCD assembly, keyboard and battery pack. (See sections 2.2.8, 2.2.2 and 2.2.1 Reassembly)

2.2.10 Inverter Board

Disassembly

1. Remove the battery, keyboard and LCD assembly. (Refer to section 2.2.1, 2.2.2 and 2.2.8 Disassembly)
2. Remove the LCD cover. (Refer to the steps 1-3 of section 2.2.9 Disassembly)
3. Remove the two screws fastening the inverter board and disconnect the cable, then free the inverter board. (Figure 2-24)

Figure 2-24 Free the inverter board

Reassembly

1. Reconnect the cable. Fit the inverter board back into place and secure with two screws.
2. Replace the LCD cover. (Refer to section 2.2.9 Reassembly)
3. Replace the LCD assembly. (Refer to section 2.2.8 Reassembly)
4. Replace the keyboard and battery pack. (Refer to sections 2.2.2 and 2.2.1 Reassembly)

2.2.11 System Board

Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, CD/DVD-ROM drive,modem card, DDR and LCD assembly. (Refer to sections 2.2.1, 2.2.2, 2 .2.3, 2.2.4, 2.2.5, 2.2.6, 2.2.7 and 2.2.8 Disassembly)
2. Disconnect the touch pad's cable from the system board. (Figure 2-25)
3. Remove the three screws fastening the housing. (Figure 2-26)

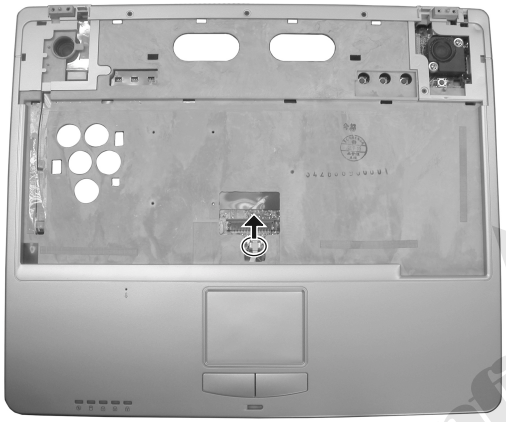


Figure 2-25 Disconnect the one cable

Figure 2-26 Remove the three screws

4. Disconnect the left speaker’s cable, then remove the twenty-one screws and free the housing. (Figure 2-27)
5. Disconnect the right speaker’s cable from the system board. (Figure 2-28)

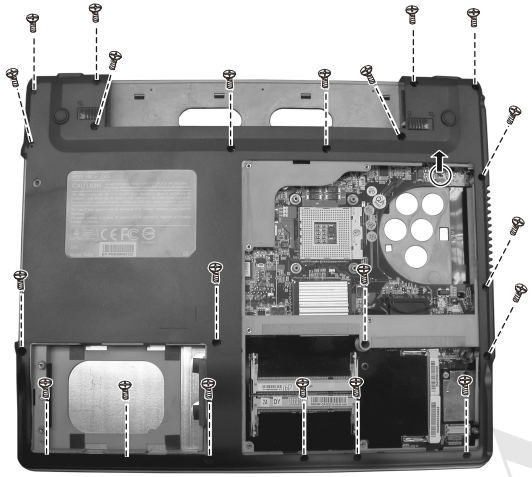


Figure 2-27 Free the housing

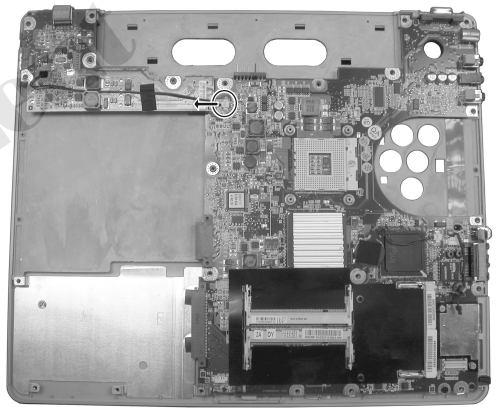


Figure 2-28 Lift the system board

6. Remove the five screws and lift the system board. (Figure 2-29)
7. Separate the daughter board from the system board and free the system board. (Figure 2-30)

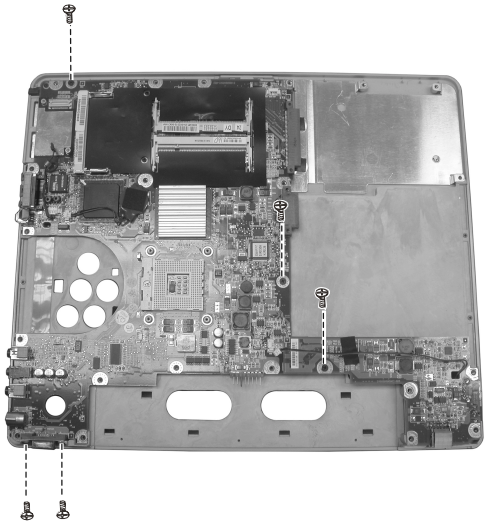


Figure 2-29 Remove the five screws

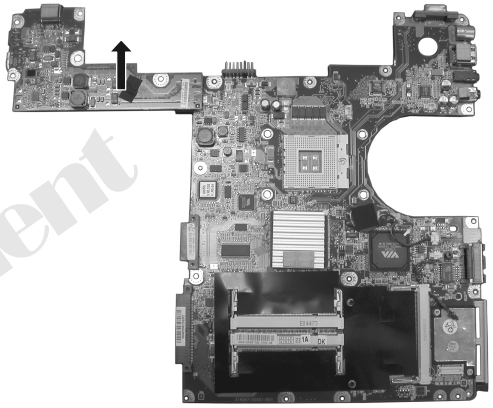


Figure 2-30 Free the system board

Reassembly

1. Replace the daughter board into the system board.
2. Replace the system board back into the top cover and secure with six screws.
3. Reconnect the right speaker’s cable into the system board.
4. Replace the housing and secure with twenty-four screws.
5. Reconnect the left speaker’s cable into the system board.
6. Turn over the base unit, then reconnect the touch pad’s cable.
7. Replace the LCD assembly, DDR, modem card, CD/DVD-ROM, hard disk drive, CPU, keyboard and battery pack. (Refer to previous section reassembly)

2.2.12 Touch Pad

Disassembly

1. Remove the battery pack, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, modem card, DDR, LCD assembly and the system board. (See sections 2.2.1, 2.2.2, 2.2.3, 2.2.4, 2.2.5, 2.2.6, 2.2.7, 2.2.8 and 2.2.11 Disassembly)
2. Remove the four screws and lift the shielding, then free the touch pad. (Figure 2-31)

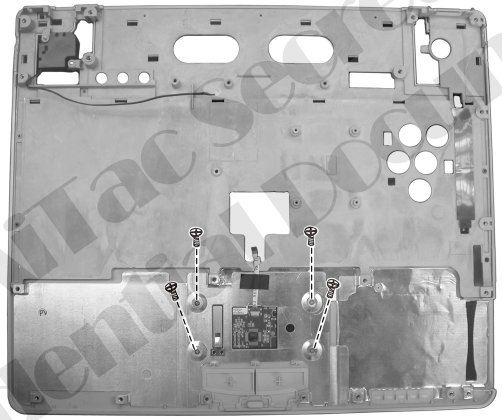


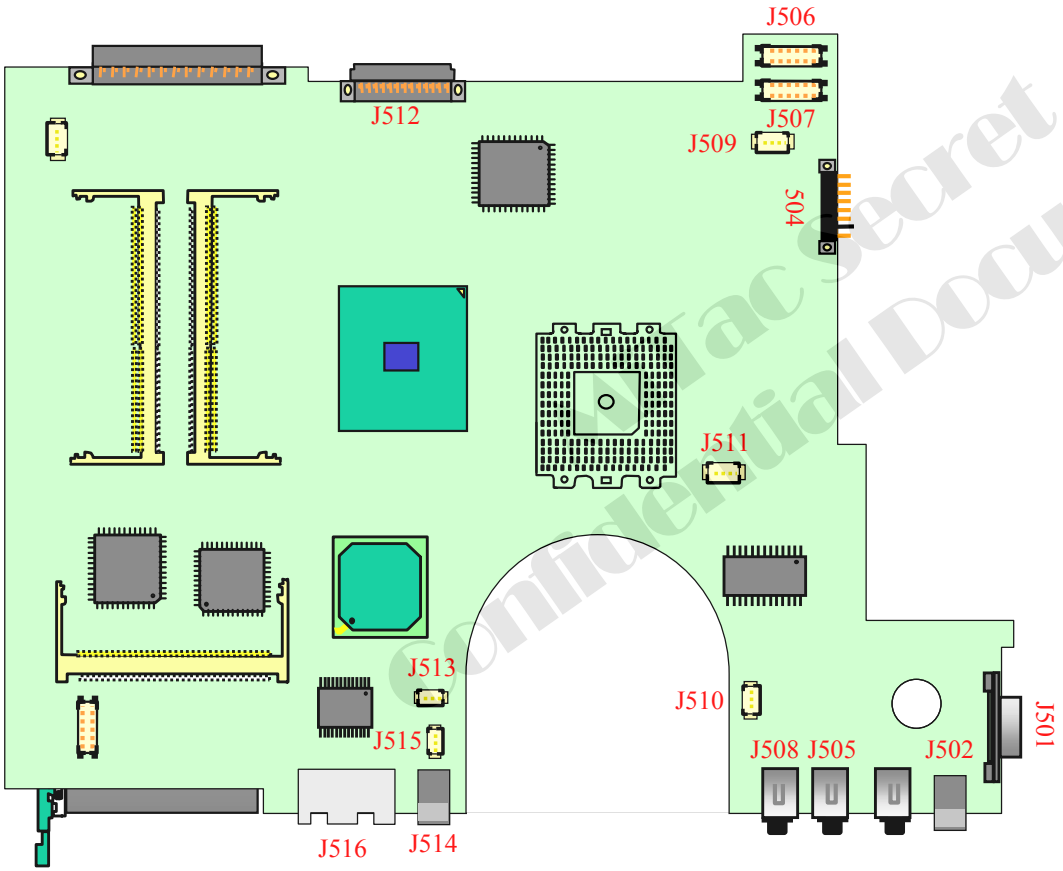
Figure 2-31 Free the touch pad

Reassembly

1. Replace the touch pad, then fit the shielding and secure with four screws.
2. Replace the battery pack, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, modem card, DDR, LCD assembly and the system board. (See sections previous section reassembly)

3. Definition & Location of Connectors / Switches

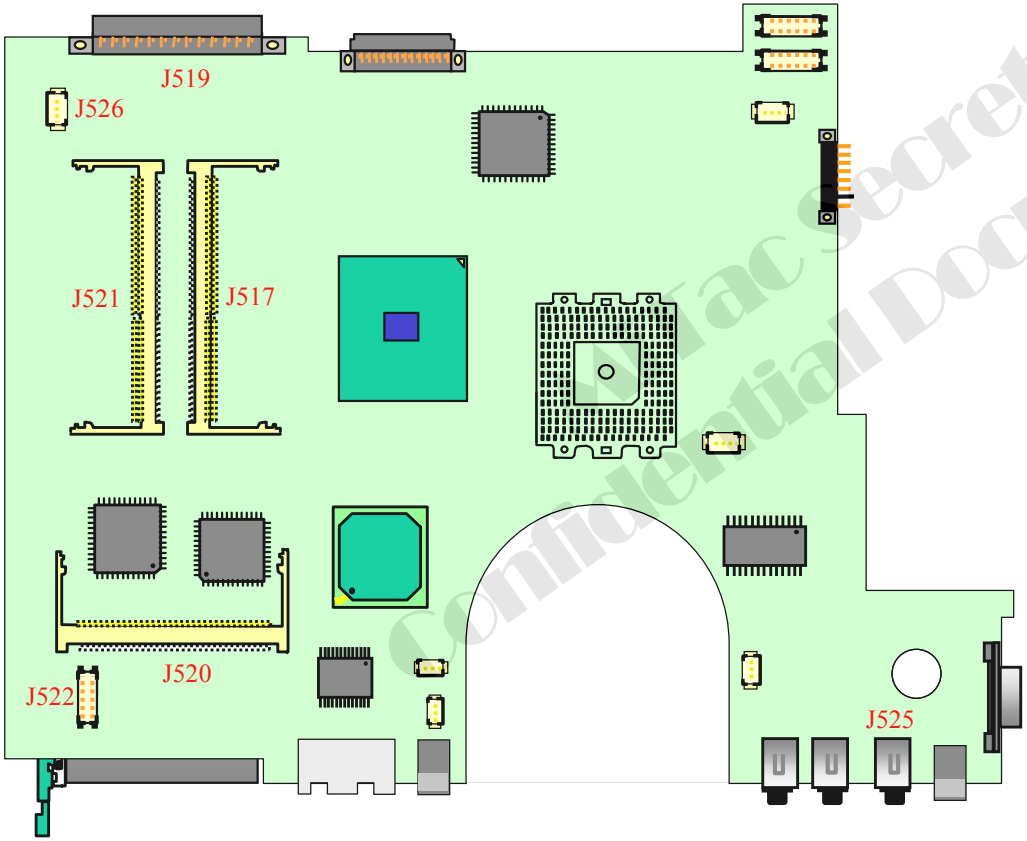
3.1 Mother Board (Side A-1)



- J501 : External VGA Connector
- J502 : S-Video Port
- J504 : Battery Connector
- J505 : S/PDIF Connector
- J506,J507 : Daughter Board Connector
- J508 : External MIC Jack
- J509 : Right Audio Channel Connector
- J510 : Left Audio Channel Connector
- J511 : CPU Fan Connector
- J512 : CD-ROM Connector
- J513 : RTC Battery Connector
- J514 : 1394 Connector
- J515 : MDC Jump Wire Connector
- J516 : RJ45&RJ11 Connector

3. Definition & Location of Connectors / Switches

3.1 Mother Board (Side A-2)



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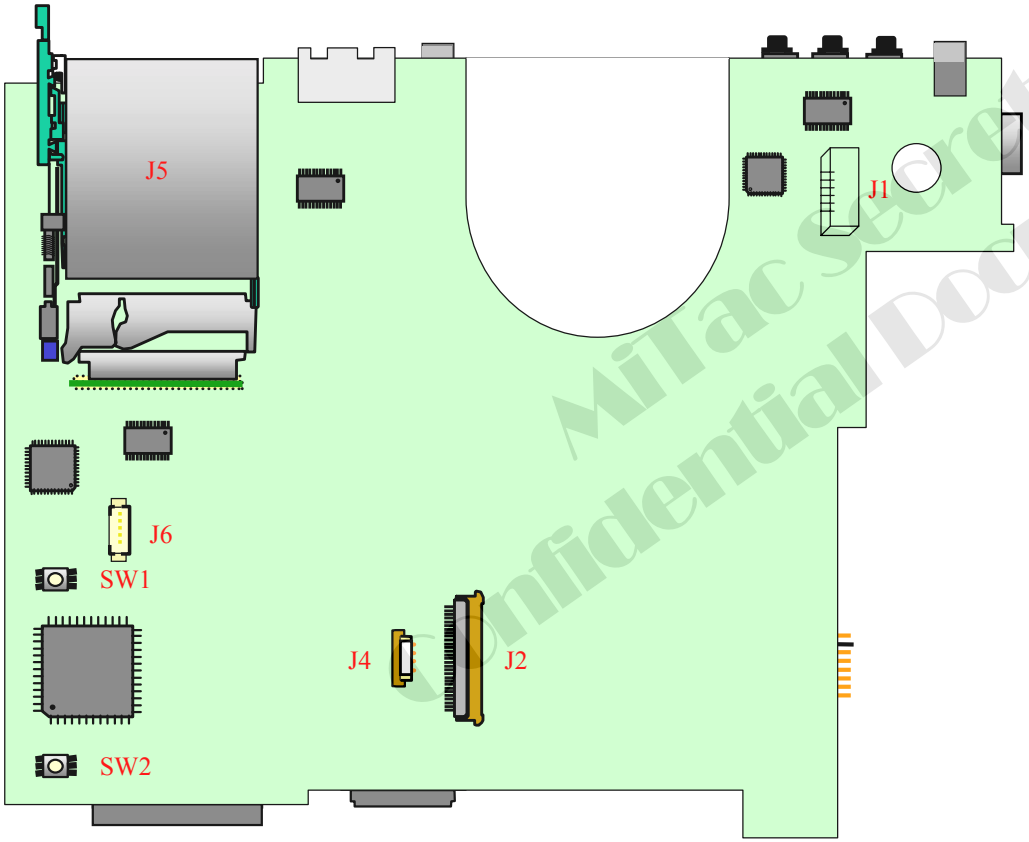
- J517,J521 : SO DIMM Slot
- J519 : HDD Connector
- J520 : MINI PCI Slot
- J522 : MDC Board Connector
- J525 : Line In Connector
- J526 : USB Interface for IR Receiver

3. Definition & Location of Connectors / Switches

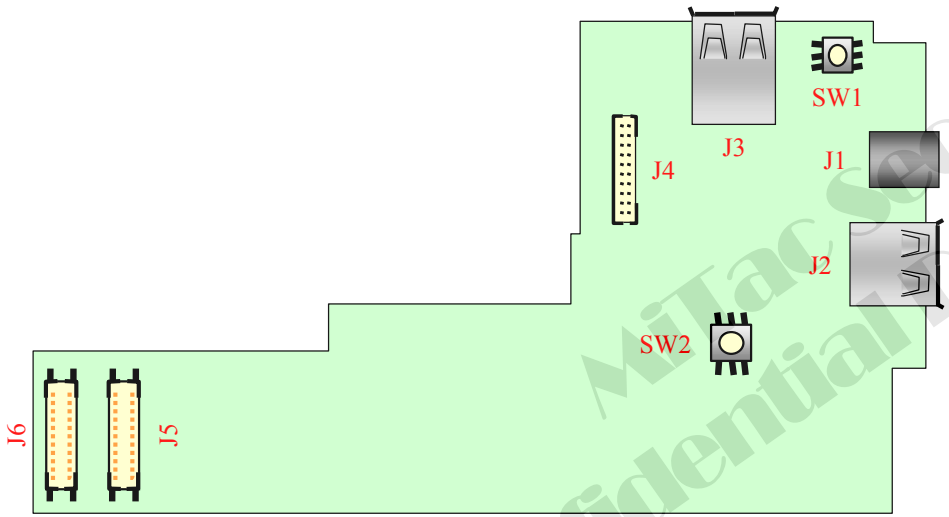
3.2 Mother Board (Side B)



- J1 : LCD Connector
- J2 : Internal Keyboard Connector
- J4 : Touch-Pad Connector
- J5 : PCMCIA Card Socket
- J6 : Blue Tooth Connector
- SW1 : Touch-Pad Left Button
- SW2 : Touch-Pad Right Button

3. Definition & Location of Connectors / Switches

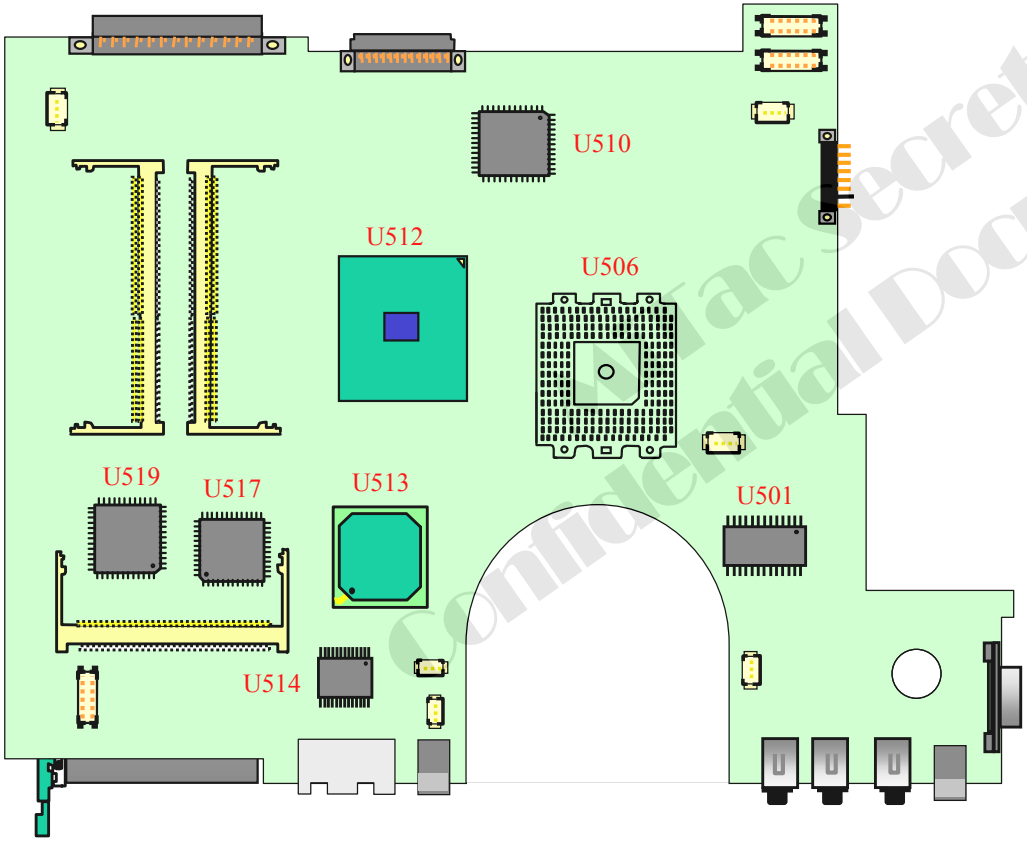
3.3 Daughter Board



- J1 : Power Jack
- J2,J3 : USB Port
- J4 : LCD Inverter Board Connector
- J5,J6 : Board to Board Connector
- SW1 : Cover Switch
- SW2 : Power Button

4. Definition & Location of Major Components

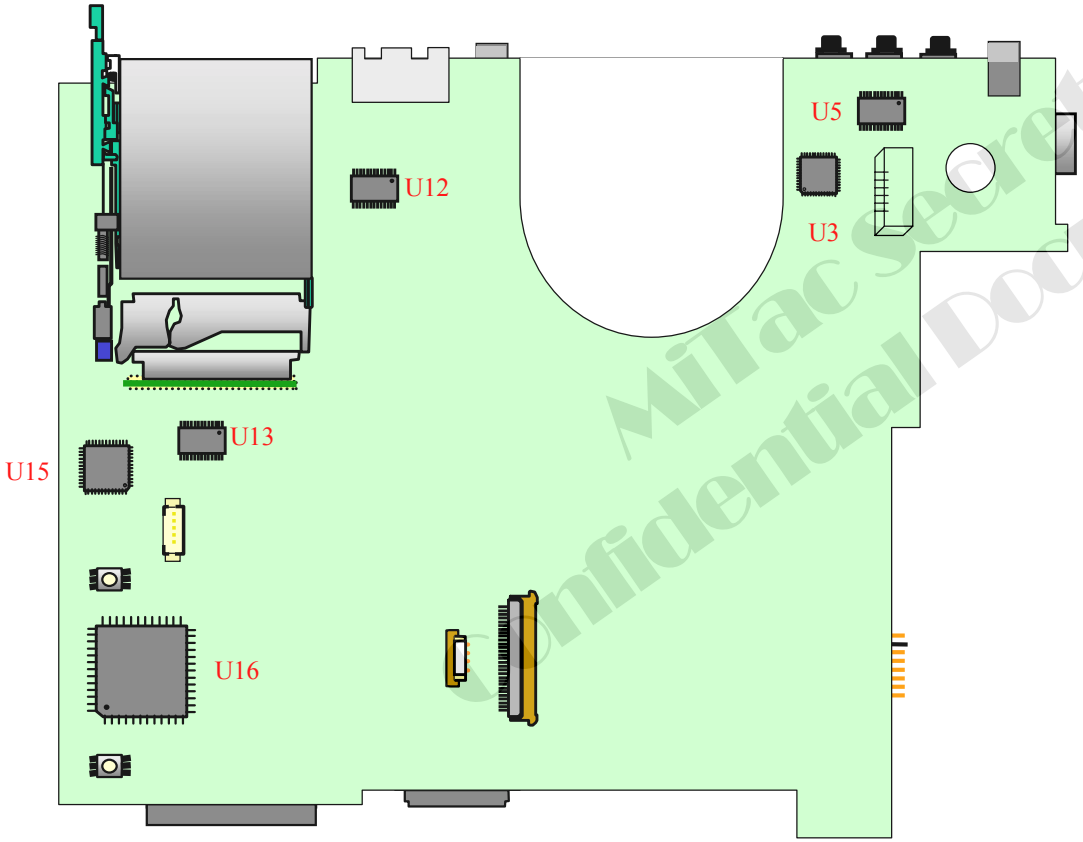
4.1 Mother Board (Side A)



- U501 : ICS954226 Clock Generator
- U506 : Intel Dothan Processor
- U510 : Windbond W83L950D Keyboard BIOS
- U512 : Intel 915GM GMCH North Bridge
- U513 : Intel ICH6-M South Bridge
- U514 : NS692403
- U517 : PCI4510GHK PCMCIA/CARDBUS
- U519 : RTL8110SBL LAN Connector

4. Definition & Location of Major Components

4.2 Mother Board (Side B)



- U3 : Audio Codec ALC655
- U5 : Amplifier TPA0212
- U13 : PCMCIA/CARDBUS Power Matrix TPS2211A
- U15 : System BIOS SST49CF004A
- U16 : PATA HDD Controller 88SA8040

5. Pin Descriptions of Major Components

5.1 Intel 915GM North Bridge(1)

Host Interface Signals

Signal Name	Type	Description
HADS#	I/O AGTL+	**Host Address Strobe:** The system bus owner asserts HADS# to indicate the first of two cycles of a request phase. The GMCH can also assert this signal for snoop cycles and interrupt messages.
HBNR#	I/O AGTL+	**Host Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
HBPRI#	O AGTL+	**Host Bus Priority Request:** The GMCH is the only Priority Agent on the system bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
HBREQ0#	I/O AGTL+	**Host Bus Request 0#:** The GMCH pulls the processor bus HBREQ**0#** signal low during HCPURST#. The signal is sampled by the processor on the active-to-inactive transition of HCPURST#. HBREQ0# should be tri-stated after the hold time requirement has been satisfied.
HCPURST#	O AGTL+	**Host CPU Reset:** The CPURST# pin is an output from the GMCH. The GMCH asserts HCPURST# while RSTIN# is asserted and for approximately 1 ms after RSTIN# is deasserted. HCPURS**T#** allows the processor to begin execution in a known state.
HDBSY#	I/O AGTL+	**Host Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
HDEFER#	O AGTL+	**Host Defer:** Signals that the GMCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.
HDINV[3:0]#	I/O AGTL+	**Host Dynamic Bus Inversion:** Driven along with the HFD[63:0]# signals. Indicates if the associated signals are inverted or not. HDINVF[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. **HDINV# Data Bits** HDINV[3]# HD[63:48]# HDINV[2]# HD[47:32]# HDINV[1]# HD[31:16]# HDINV[0]# HD[15:0]#

Host Interface Signals (Continued)

Signal Name	Type	Description
HDRDY#	I/O AGTL+	**Host Data Ready:** Asserted for each cycle that data is transferred.
HA[31:3]#	I/O AGTL+ 2X	**Host Address Bus:** HA[31:3]# connects to the CPU address bus. During processor cycles the HA[31:3]# are inputs. The GMCH drives HA[31:3]# during snoop cycles on behalf of DMI. HA[31:3]# are transferred at 2x rate. Note that the address is inverted on the CPU bus.
HADSTB[1:0]#	I/O AGTL+ 2X	**Host Address Strobe:** HA[31:3]# connects to the CPU address bus. During CPU cycles, the source synchronous strobes are used to transfer HA[31:3]# and HREQ[4:0]# at the 2x transfer rate. **Strobe Address Bits** HADSTB[0]# HA[16:3]#, HREQ[4:0]# HADSTB[1]# HA[31:17]#
HD[63:0]#	I/O AGTL+ 4X	**Host Data:** These signals are connected to the CPU data bus. HD[63:0]# are transferred at 4x rate. Note that the data signals are inverted on the CPU bus depending on the HDINV[3:0]# signals.
HDSTBP[3:0]# HDSTBN[3:0]#	I/O AGTL+ 4X	**Host Differential Host Data Strobes:** The differential source synchronous strobes are used to transfer HD[63:0]# and HDINV[3:0]# at the 4x transfer rate. **Strobe Data Bits** HDSTBP[3]#, HDSTBN[3]# HD[63:48]#, HDINV[3]# HDSTBP[2]#, HDSTBN[2]# HD[47:32]#, HDINV[2]# HDSTBP[1]#, HDSTBN[1]# HD[31:16]#, HDINV[1]# HDSTBP[0]#, HDSTBN[0]# HD[15:00]#, HDINV[0]#
HHIT#	I/O AGTL+	**Host Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HITM# by the target to extend the snoop window.
HHITM#	I/O AGTL+	**Host Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop window.

5.1 Intel 915GM North Bridge(2)

Host Interface Signals (Continued)

Signal Name	Type	Description
HLOCK#	I AGTL+	**Host Lock:** All CPU bus cycles sampled with the assertion of HLOCK# and HADS#, until the negation of HLOCK# must be atomic, i.e. *PCI Express graphics access* to System Memory is allowed when HLOCK# is asserted by the CPU.
HREQ[4:0]#	I/O AGTL+ 2X	**Host Request Command:** Defines the attributes of the request. HREQ[4:0]# are transferred at 2x rate. Asserted by the requesting agent during both halves of the Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type.
HTRDY#	O AGTL+	**Host Target Ready:** Indicates that the target of the processor transaction is able to enter the data transfer phase.
HRS[2:0]#	O AGTL+	**Host Response Status:** Indicates the type of response according to the following the table: **HRS[2:0]# Response type** 000 Idle state 001 Retry response 010 Deferred response 011 Reserved (not driven by GMCH) 100 Hard Failure (not driven by GMCH) 101 No data response 110 Implicit Write back 111 Normal data response
HDPWR#	O AGTL+	**Host Data Power:** Used by GMCH to indicate that a data return cycle is pending within 2 HCLK cycles or more. CPU use's this signal during a read-cycle to activate the data input buffers in preparation for HDRDY# and the related data.
HCPUSLP#	O CMOS	**Host CPU Sleep:** When asserted in the Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts.

Host Interface Reference and Compensation

Signal Name	Type	Description
HVREF	I A	**Host Reference Voltage:** Reference voltage input for the Data, Address, and Common clock signals of the Host AGTL+ interface.
HXRCOMP	I/O A	**Host X RCOMP:** Used to calibrate the Host AGTL+ I/O buffers. This signal is powered by the Host Interface termination rail (VCCP).
HXSCOMP	I/O A	**Host X SCOMP**: Slew Rate Compensation for the Host Interface
HXSWING	I A	**Host X Voltage Swing:** These signals provide reference voltages used by the HXRCOMP circuits.
HYRCOMP	I/O A	**Host Y RCOMP**: Used to calibrate the Host AGTL+ I/O buffers.
HYSCOMP	I/O A	**Host Y SCOMP:** Slew Rate Compensation for the Host Interface
HYSWING	I A	**Host Y Voltage Swing:** These signals provide reference voltages used by the HYRCOMP circuitry.

DMI

Signal Name	Type	Description
DMI_RXP[1:0] DMI_RXN[1:0]	I PCIE	**DMI input from ICH6-M:** Direct Media Interface receive differential pair
DMI_TXP[1:0] DMI_TXN[1:0]	O PCIE	**DMI output to ICH6-M:** Direct Media Interface transmit differential pair

DMI x2 is supported for Intel 915GMS chipset

5.1 Intel 915GM North Bridge(3)

DDR / DDR2 SDRAM Channel A Interface

Signal Name	Type	Description
SA_DQ[63:0]	I/O SSTL1.8/2 2x	**Data Bus:** DDR / DDR2 Channel A data signal interface to the SDRAM data bus. Single channel mode: Route to SO-DIMM 0 & SO-DIMM1 Dual channel mode: Route to SO-DIMM A
SA_DM[7:0]	I/O SSTL1.8/2 2x	**Data Mask:** These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes. When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SA_DM[7:0] for every data byte lane. Single channel mode: Route to SO-DIMM 0 & SO-DIMM1 Dual channel mode: Route to SO-DIMM A
SA_DQS[7:0]	I/O SSTL1.8 2x	**Data Strobes:** DDR: The rising and falling edges of SA_DQS[7:0] are used for capturing data during read and write transactions. DDR2: SA_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SA_DQS[7:0] and its SA_DQS[7:0]# during read and write transactions. Single channel mode: Route to SO-DIMM 0 & SO-DIMM1 Dual channel mode: Route to SO-DIMM A
SA_DQS[7:0]#	I/O SSTL1.8 2x	**Data Strobe Complements** DDR1: No Connect. These signals are not used for DDR devices DDR2 : These are the complementary DDR2 strobe signals. Single channel mode: Route to SO-DIMM 0 & SO-DIMM1 Dual channel mode: Route to SO-DIMM A
SA_MA[13:0]	O SSTL1.8/2	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A Note: SA_MA13 is for support of 1 Gb devices.
SA_BS[2:0]	O SSTL1.8/2	**Bank Selec**t: These signals define which banks are selected within each SDRAM rank. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A Note: SA_BS2 is for support for DDR2 only for 8 bank devices.

DDR / DDR2 SDRAM Channel A Interface (Continued)

Signal Name	Type	Description
SA_RAS#	O SSTL1.8/2	**RAS Control signa**l: Used with SA_CAS# and SA_WE# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A
SA_CAS#	O SSTL1.8/2	**CAS Control signal:** Used with SA_RAS# and SA_WE# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A
SA_WE#	O SSTL1.8/2	**Write Enable Control signal:** Used with SA_RAS# and SA_CAS# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A
SA_RCVENIN#	O SSTL1.8/2	**Clock Input:** Used to emulate source-synch clocking for reads. Connects internally to SA_RCVENOUT#. Leave as No Connect.
SA_RCVENOUT#	O SSTL1.8/2	**Clock Output:** Used to emulate source-synch clocking for reads. Connects internally to SA_RCVENIN#. Leave as No Connect.

PCI Express Based Graphics Interface Signals

Signal Name	Type	Description
EXP_RXN[15:0] EXP_RXP[15:0]	I PCIE	PCI Express Receive Differential Pair
EXP_TXN[15:0] EXP_TXP[15:0]	O PCIE	PCI Express Transmit Differential Pair
EXP_ICOMPO	I A	PCI Express Output Current and Resistance Compensation
EXP_COMPI	I A	PCI Express Input Current Compensation

PCI Express Based Graphics is supported for Intel 915GM and Intel 915PM chipsets.

5.1 Intel 915GM North Bridge(4)

DDR / DDR2 SDRAM Channel B Interface

Signal Name	Type	Description
SB_DQ[63:0]	I/O SSTL1.8/2 2x	**Data Line**s: DDR / DDR2 Channel B data signal interface to the SDRAM data bus. Single Channel mode: No connect. Dual channel mode: Route to SO-DIMM B **NOT**E: Signals do not exist in Intel 915GMS.
SB_DM[7:0]	O SSTL1.8/2 2x	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SB_DM[7:0] for every data byte lane. These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes. Single Channel mode: No connect. Dual channel mode: Route to SO-DIMM B **NOT**E: Signals do not exist in Intel 915GMS.
SB_DQS[7:0]	I/O SSTL1.8/2 2x	**Data Strobes:** DDR: The rising and falling edges of SB_DQS[7:0] are used for capturing data during read and write transactions. DDR2: SB_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SB_DQS[7:0] and its SB_DQS[7:0]# during read and write transactions. Single Channel mode: No connect. Dual channel mode: Route to SO-DIMM B **NOT**E: Signals do not exist in Intel 915GMS.
SB_DQS[7:0]#	I/O SSTL1.8 2x	**Data Strobe Complements** (DDR2 only): DDR1: No Connect. These signals are not used for DDR devices DDR2 : These are the complementary DDR2 strobe signals. Single Channel mode: No connect. Dual channel mode: Route to SO-DIMM B **NOT**E: Signals do not exist in Intel 915GMS.
SB_MA[13:0]	O SSTL1.8/2	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B **NOT**E: SB_MA13 is for support of 1 Gb devices.
SB_BS[2:0]	O SSTL1.8/2	**Bank Selec**t: These signals define which banks are selected within each SDRAM rank. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B **NOT**E: SB_BS2 is for DDR2 support only.

DDR / DDR2 SDRAM Channel B Interface (Continued)

Signal Name	Type	Description
SB_RAS#	O SSTL1.8/2	**RAS Control signa**l: Used with SB_CAS# and SB_WE# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B
SB_CAS#	O SSTL1.8/2	**CAS Control signal:** Used with SB_RAS# and SB_WE# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B
SB_WE#	O SSTL1.8/2	**Write Enable Control signal:** Used with SB_RAS# and SB_CAS# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B
SB_RCVENIN#	I SSTL1.8/2	**Clock Input:** Used to emulate source-synch clocking for reads. Leave as No Connect. **NOT**E: Signals do not exist in Intel 915GMS.
SB_RCVENOUT#	O SSTL1.8/2	**Clock Output:** Used to emulate source-synch clocking for reads. Leave as No Connect. **NOT**E: Signals do not exist in Intel 915GMS.

DMI

Signal Name	Type	Description
DMI_RXP[3:0] DMI_RXN[3:0]	I PCIE	**DMI input from ICH6-M:** Direct Media Interface receive differential pair
DMI_TXP[3:0] DMI_TXN[3:0]	O PCIE	**DMI output to ICH6-M:** Direct Media Interface transmit differential pair

DMI x2 or x4 is supported for Intel 915GM, Intel 915PM and Intel 910GML chipsets.

5.1 Intel 915GM North Bridge(5)

DDR / DDR2 Common Signals

Signal Name	Type	Description
SM_CK[1:0], SM_CK[4:3]	O SSTL1.8/2	**SDRAM Differential Clock:** The crossing of the positive edge of SM_CKx and the negative edge of its complement SM_CKx# are used to sample the command and control signals on the SDRAM. **SM_CK[0:1]** and its complement **SM_CK[1:0]#** signal make a differential clock pair output. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A **SM_CK[4:3]** and its complement **SM_CK[4:3]#** signal make a differential clock pair output. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B **NOT**E: **SM_CK2** and **SM_CK5** are reserved and not supported.
SM_CK[1:0]#, SM_CK[4:3]#	O SSTL1.8/2	**SDRAM Inverted Differential Clock:** These are the complementary Differential DDR2 Clock signals. **NOT**E: **SM_CK2#** and **SM_CK5#** are reserved and not supported.
SM_CS[3:0]#	O SSTL1.8/2	**Chip Select:** (1 per Rank): These signals select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank **SM_CS[1:0]#** : Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A **SM_CS[3:2]#** : Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B
SM_CKE[3:0]	O SSTL1.8/2	**Clock Enable:** (1 per Rank): SM_CKE[3:0] is used: .To initialize the SDRAMs during power-up .To power-down SDRAM ranks . To place all SDRAM ranks into and out of self-refresh during STR. SM_CKE[1:0]: Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A SM_CKE[3:2]: Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B

DDR / DDR2 Common Signals (Continued)

Signal Name	Type	Description
SM_ODT[3:0]	O SSTL1.8/2	**On Die Termination: Active Termination Contro**l. (DDR2 only) SM_ODT[1:0]: Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A *Signal Description* The crossing of the positive edge of SM_CKx and the negative edge of its complement SM_CKx# are used to sample the command and control **SM_CK[0:1]** and its complement **SM_CK[1:0]#** signal make a differential **SM_CK[4:3]** and its complement **SM_CK[4:3]#** signal make a differential **NOT**E: **SM_CK2** and **SM_CK5** are reserved and not supported. These are the complementary Differential DDR2 Clock signals. **NOT**E: **SM_CK2#** and **SM_CK5#** are reserved and not supported. These signals select particular SDRAM components during the active To place all SDRAM ranks into and out of self-refresh during STR. **On Die Termination: Active Termination Contro**l. (DDR2 only) SM_ODT[3:2]: Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B DDR: Leave as no connects. Not used for DDR devices. DDR2: On-die termination for DDR2 devices.

5.1 Intel 915GM North Bridge(6)

CRT DAC Signals

Signal Name	Type	Description
RED	O A	**RED Analog Video Output**: This signal is a CRT Analog video output from the internal color palette DAC.
RED#	O A	**RED# Analog Output**: This signal is an analog video output from the internal color palette DAC. This signal is used to provide noise immunity.
GREEN	O A	**GREEN Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC.
GREEN#	O A	**GREEN# Analog Output**: This signal is an analog video output from the internal color palette DAC. This signal is used to provide noise immunity.
BLUE	O A	**BLUE Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC.
BLUE#	O A	**BLUE# Analog Output:** This signal is an analog video output from the internal color palette DAC. This signal is used to provide noise immunity.
REFSET	O A	**Resistor Set**: Set point resistor for the internal color palette DAC. A 256-Ω ± 1% resistor is required between REFSET and motherboard ground.
HSYNC	O HVCMOS	**CRT Horizontal Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or “sync interval”.
VSYNC	O HVCMOS	**CRT Vertical Synchronization**: This signal is used as the vertical sync (polarity is programmable).

Analog TV-out Signals

Signal Name	Type	Description
TVDAC_A	O A	**TVDAC Channel A Output:** TVDAC_A supports the following: **Composite**: CVBS signal **Component**: Chrominance (Pb) analog signal
TVDAC_B	O A	**TVDAC Channel B Output:** TVDAC_B supports the following: **S-Video**: Luminance analog signal **Component**: Luminance (Y) analog signal
TVDAC_C	O A	**TVDAC Channel C Output:** TVDAC_C supports the following: **S-Video**: Chrominance analog signal **Component**: Chrominance (Pr) analog signal
TV_IRTNA	O A	**Current Return for TVDAC Channel A:** Connect to ground on board
TV_IRTNB	O A	**Current Return for TVDAC Channel B:** Connect to ground on board
TV_IRTNC	O A	**Current Return for TVDAC Channel C:** Connect to ground on board
TV_REFSET	O A	**TV Resistor set:** TV Reference Current uses an external resistor to set internal reference voltage levels. A 5-k §Ù ± 0.5% resistor is required between REFSET and motherboard ground.

5.1 Intel 915GM North Bridge(7)

Display Data Channel (DDC) and GMBUS Support

Signal Name	Type	Description
LCTLA_CLK	I/O COD	I2C Based control signal (Clock) for External SSC clock chip control –
LCTLB_DATA	I/O COD	I2C Based control signal (Data) for External SSC clock chip control –
DDCCLK	I/O COD	CRT DDC clock monitor control support
DDCDATA	I/O COD	CRT DDC Data monitor control support
LDDC_CLK	I/O COD	EDID support for flat panel display
LDDC_DATA	I/O COD	EDID support for flat panel display
SDVOCTRL_CLK	I/O COD	I2C Based control signal (Clock) for SDVO device
SDVOCTRL_DATA	I/O COD	I2C Based control signal (Data) for SDVO device

DDR SDRAM Reference and Compensation

Signal Name	Type	Description
SMRCOMPN	I/O A	**System Memory RCOMP** N: Buffer compensation This signal is powered by the System Memory rail (2.5 V for DDR, 1.8 V for DDR2).
SMRCOMPP	I/O A	**System Memory RCOMP** P: Buffer compensation This signal is powered by the System Memory rail
SMXSLEWIN	I A	**X Buffer Slew Rate Input control.**
SMXSLEWOUT	O A	**X Buffer Slew Rate Output control.**
SMYSLEWIN	I A	**Y Buffer Slew Rate Input control.**
SMYSLEWOUT	O A	**Y Buffer Slew Rate Output control.**
SMVREF[1:0]	I A	**SDRAM Reference Voltage:** Reference voltage inputs for each DQ, DQS, & RCVENIN#. Also used during ODT RCOMP.
SMOCDCOMP[1:0]	I A	**On-Die DRAM OCD driver compensation** OCD compensation

LVDS Signals

Signal Name	Type	Description
LDVS Channel A		
LADATAP[2:0]	I/O LVDS	Channel A differential data output - positive
LADATAN[2:0]	I/O LVDS	Channel A differential data output –negative
LACLKP	I/O LVDS	Channel A differential clock output – positive
LACLKN	I/O LVDS	Channel A differential clock output – negative
LDVS Channel B		
LBDATAP[2:0]	I/O LVDS	Channel B differential data output – positive **NOT**E: Signals do not exist in Intel 915GMS.
LBDATAN[2:0]	I/O LVDS	Channel B differential data output –negative **NOT**E: Signals do not exist in Intel 915GMS.
LBCLKP	I/O LVDS	Channel B differential clock output – positive **NOT**E: Signals do not exist in Intel 915GMS.
LBCLKN	I/O LVDS	Channel B differential clock output – negative **NOT**E: Signals do not exist in Intel 915GMS.
LFP Panel power and backlight control		
LVDD_EN	O HVCMOS	LVDS panel power enable: Panel power control enable control. This signal is also called VDD_DBL in the CPIS specification and is used to control the VDC source to the panel logic.
LBKLT_EN	O HVCMOS	LVDS backlight enable: Panel backlight enable control. This signal is also called ENA_BL in the CPIS specification and is used to gate power into the backlight circuitry.
LBKLT_CRTL	O HVCMOS	Panel backlight brightness control: Panel brightness control. This signal is also called VARY_BL in the CPIS specification and is used as the PWM Clock input signal.
LVDS Reference signals		
LIBG	I/O Ref	LVDS Reference Current. – 1.5 kΩ Pull down resistor needed
LVREFH	I Ref	Reserved. - No connect.
LVREFL	I Ref	Reserved. - No connect.
LVBG	O A	Reserve. - No connect

Note: LVDS Channel B interface is not supported and do not exist for Intel 915GMS

5.1 Intel 915GM North Bridge(8)

Serial DVO Interface.

Signal Name	Type	Description
SDVO B Interface		
SDVOB_CLKP	O PCIE	Serial Digital Video B Clock. Multiplexed with EXP_TXP_3.
SDVOB_CLKN	O PCIE	Serial Digital Video B Clock Complement. Multiplexed with EXP_TXN_3.
SDVOB_RED	O PCIE	Serial Digital Video B Red Data. Multiplexed with EXP_TXP_0.
SDVOB_RED#	O PCIE	Serial Digital Video B Red Data Complement. Multiplexed with EXP_TXN_0.
SDVOB_GREEN	O PCIE	Serial Digital Video B Green Data. Multiplexed with EXP_TXP_1.
SDVOB_GREEN#	O PCIE	Serial Digital Video B Green Data Complement. Multiplexed with EXP_TXN_1.
SDVOB_BLUE	O PCIE	Serial Digital Video B Blue Data. Multiplexed with EXP_TXP_2.
SDVOB_BLUE#	O PCIE	Serial Digital Video B Blue Data Complement. Multiplexed with EXP_TXN_2.
SDVO C Interface		
SDVOC_RED	O PCIE	Serial Digital Video C Red Data / SDVO B Alpha. Multiplexed with EXP_TXP_4. **NOT**E: Signals do not exist in Intel 915GMS..
SDVOC_RED#	O PCIE	Serial Digital Video C Red Complement / Alpha Complement. Multiplexed with EXP_TXN_4. **NOT**E: Signals do not exist in Intel 915GMS.
SDVOC_GREEN	O PCIE	Serial Digital Video C Green. Multiplexed with EXP_TXP_5. **NOT**E: Signals do not exist in Intel 915GMS.
SDVOC_GREEN#	O PCIE	Serial Digital Video C Green Complement. Multiplexed with EXP_TXN_5. **NOT**E: Signals do not exist in Intel 915GMS.
SDVOC_BLUE	O PCIE	Serial Digital Video Channel C Blue. Multiplexed with EXP_TXP_6. **NOT**E: Signals do not exist in Intel 915GMS.
SDVOC_BLUE#	O PCIE	Serial Digital Video C Blue Complement. Multiplexed with EXP_TXN_6. **NOT**E: Signals do not exist in Intel 915GMS.

Serial DVO Interface (Continued)

Signal Name	Type	Description
SDVO C Interface		
SDVOC_CLKP	O PCIE	Serial Digital Video C Clock. Multiplexed with EXP_TXP_7. **NOT**E: Signals do not exist in Intel 915GMS.
SDVOC_CLKN	O PCIE	Serial Digital Video C Clock Complement. Multiplexed with EXP_TXN_7. **NOT**E: Signals do not exist in Intel 915GMS.
SDVO Common Signals		
SDVO_TVCLKIN	I PCIE	Serial Digital Video TVOUT Synchronization Clock. Multiplexed with EXP_RXP_0.
SDVO_TVCLKIN#	I PCIE	Serial Digital Video TV-out Synchronization Clock Complement. Multiplexed with EXP_RXN_0.
SDVO_FLDSTALL	I PCIE	Serial Digital Video Field Stall. Multiplexed with EXP_RXP_2.
SDVO_FLDSTALL#	I PCIE	Serial Digital Video Field Stall Complement. Multiplexed with EXP_RXN_2.
SDVOB_INT	I PCIE	Serial Digital Video Input Interrupt. Multiplexed with EXP_RXP_1.
SDVOB_INT#	I PCIE	Serial Digital Video Input Interrupt Complement. Multiplexed with EXP_RXN_1.
SDVOC_INT	I PCIE	Serial Digital Video Input Interrupt. Multiplexed with EXP_RXP_5.
SDVOC_INT#	I PCIE	Serial Digital Video Input Interrupt Complement. Multiplexed with EXP_RXN_5.

5.1 Intel 915GM North Bridge(9)

Reset and Miscellaneous Signals

Signal Name	Type	Description
RSTIN#	I HVCMOS	**Reset In**: When asserted this signal will asynchronously reset the GMCH logic. This signal is connected to the PLT_RST# output of the ICH6-M. This input has a Schmitt trigger to avoid spurious resets. This input buffer is 3.3-V tolerant.
PWROK	I HVCMOS	**Power OK**: When asserted, PWROK is an indication to the GMCH that core power has been stable for at least 10 µs. This input buffer is 3.3-V tolerant.
H_BSEL [2:0] (CFG[2:0])	I HVCMOS	**Host Bus Speed Select:** At the deassertion of RSTIN#, the value sampled on these pins determines the expected frequency of the bus. External pull-ups are required.
CFG[17:3]	I AGTL+	**HW straps:** CFG [17:3] has internal pull up. **NOT**E: Not all CFG Balls are supported for Intel 915GMS.
CFG[20:18]	I HVCMOS	**HW straps:** CFG [20:18] has internal pull down **NOT**E: Not all CFG Balls are supported for Intel 915GMS.
BM_BUSY#	O HVCMOS	**GMCH Integrated Graphics Bus**y: Indicates to the ICH that the integrated graphics engine within the MCH is busy and transitions to low power states should not be attempted until that is no longer the case.
THRMTRIP#	O COD	**GMCH Thermal Tri**p: Assertion of THERMTRIP# (Thermal Trip) indicates the GMCH junction temperature has reached a level beyond which damage may occur. Upon assertion of THERMTRIP#, the GMCH will shut off its internal clocks (thus halting program execution) in an attempt to reduce the GMCH core junction temperature. To protect GMCH, its core voltage (Vcc) must be removed following the assertion of THERMTRIP#. Once activated, THERMTRIP# remains latched until RSTIN# is asserted. While the assertion of the RSTIN# signal will deassert THERMTRIP#, if the GMCH's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted.
EXT_TS[1:0]#	I HVCMOS	**External Thermal Sensor Input**: If the system temperature reaches a dangerously high value then this signal can be used to trigger the start of system memory throttling. **NOT**E: EXT_TS1# functionality is not supported in 915GMS. A pull up is required on this pin

PLL Signals

Signal Name	Type	Description
HCLKP	I Diff Clk	**Differential Host Clock In**: Differential clock input for the Host PLL. Used for phase cancellation for FSB transactions. This clock is used by all of the GMCH logic that is in the Host clock domain. Also used to generate core and system memory internal clocks. This is a low voltage differential signal and runs at ¼ the FSB data rate.
HCLKN	I Diff Clk	**Differential Host Clock Input Complement:**
GCLKP	I Diff Clk	**Differential PCI Express based Graphics / DMI Clock In**: These pins receive a differential 100 MHz Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express.
GCLKN	I Diff Clk	**Differential PCI Express based Graphics / DMI Clock In complement**
DREF_CLKP	I Diff Clk	**Display PLLA Differential Clock In** – Display PLL Differential Clock In, no SSC support –
DREF_CLKN	I Diff Clk	**Display PLLA Differential Clock In Complement** – Display PLL Differential Clock In Complement - no SSC support
DREF_SSCLKP	I Diff Clk	**Display PLLB Differential Clock In** – Optional Display PLL Differential Clock In for SSC support – **NOT**E: Differential Clock input for optional SSC support for LVDS display.
DREF_SSCLKN	I Diff Clk	**Display PLLB Differential Clock In complement** – Optional Display PLL Differential Clock In Complement for SSC support **NOT**E: Differential Clock input for optional SSC support for LVDS display.

Note: PLL interfaces signal group are supported the Mobile Intel 915GM/PM/GMS and Intel 910GML Express chipsets, unless otherwise noted.

5.1 Intel 915GM North Bridge(10)

Power and Ground

Interface	Ball Name	Description
Host	VTT (VCCP)	FSB power supply (1.05 V) - (VCCP)
DRAM	VCCA_SM	VCCASM is the Analog power supply for SM data buffers used for DLL & other logic (1.5 V)
	VCCSM	System memory power supply (DDR=2.5 V; DDR2=1.8 V)
PCI Express Based Graphics /DMI	VCC3G	PCI Express / DMI Analog power supply (1.5 V)
	VCCA_3GBG	PCI Express / DMI band gap power supply (2.5 V)
	VSSA_3GBG	PCI Express / DMI band gap ground
PLL Analog	VCCA_HPLL	Power supply for the Host VCO in the host/mem/core PLL (1.5 V)
	VCCA_MPLL	Power supply for the mem VCO in the host/mem/core PLL (1.5 V)
	VCCD_HMPLL	Power Supply for the digital dividers in the HMPLL (1.5 V)
	VCCA_3GPLL	Power supply for the 3GIO PLL (1.5 V)
	VCCA_DPLLA	Display A PLL power supply (1.5 V)
	VCCA_DPLLB	Display B PLL power supply (1.5 V)
High Voltage Interfaces	VCCHV	Power supply for the HV buffers (2.5 V)
CRT DAC	VCCA_CRTDAC	Analog power supply for the DAC (2.5 V)
	VSSA_CRTDAC	Analog ground for the DAC
	VCC_SYNC	Power supply for HSYNC/ VSYNC (2.5 V)
LVDS	VCCD_LVDS	Digital power supply (1.5 V)
	VCCTX_LVDS	Data/Clk Tx power supply (2.5 V)
	VCCA_LVDS	LVDS analog power supply (2.5 V)
	VSSALVDS	LVDS analog VSS

Power and Ground (Continued)

Interface	Ball Name	Description
TVDAC	VCCA_TVBG	TV DAC Band Gap Power (3.3 V)
	VSSA_TVBG	TV DAC Band Gap VSS
	VCCD_TVDAC	Dedicated Power Supply for TVDAC (1.5 V)
	VCCDQ_TVDAC	Power Supply for Digital Quiet TVDAC (1.5 V)
	VCCA_TVDACA	Power Supply for TV Out Channel A (3.3 V)
	VCCA_TVDACB	Power Supply for TV Out Channel B (3.3 V)
	VCCA_TVDACC	Power Supply for TV Out Channel C (3.3 V)
Core	VCC	Core VCC – (1.05 V or 1.5 V)
Ground	VSS	Ground
NCTF	**Non-Critical To Function power signals:** "NCTF" (Non-Critical To Function) have been designed into the package footprint to enhance the Solder Joint Reliability of our products by absorbing some of the stress introduced by the Characteristic Thermal Expansion (CTE) mismatch of the Die to package interface. It is expected that in some cases, these balls may crack partially or completely, however, this will have no impact to our product performance or reliability. Intel has added these balls primarily to serve as sacrificial stress absorbers. **NOT**E: Signals do not exist in Intel 915GMS.	
	VTT_NCTF	NCTF FSB power supply (1.05 V or 1.2 V)
	VCC_NCTF	NTCF Core VCC – (1.05 V or 1.5 V)
	VCCSM_NCTF	NTCF System memory power supply (DDR=2.5 V; DDR2=1.8 V)
	VSS_NCTF	NTCF Ground

5.2 Intel ICH6-M South Bridge(1)

PCI Interface Signals

Name	Type	Description
AD[31:0]	I/O	**PCI Address/Data**: AD[31:0] is a multiplexed address and data bus. During the first clock of a transaction, AD[31:0] contain a physical address (32 bits). During subsequent clocks, AD[31:0] contain data. The Intel® ICH6 will drive all 0s on AD[31:0] during the address phase of all PCI Special Cycles.
C/BE[3:0]#	I/O	**Bus Command and Byte Enable**s: The command and byte enable signals are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# define the Byte Enables. **C/BE[3:0]# Command Type** 0000b Interrupt Acknowledge 0001b Special Cycle 0010b I/O Read 0011b I/O Write 0110b Memory Read 0111b Memory Write 1010b Configuration Read 1011b Configuration Write 1100b Memory Read Multiple 1110b Memory Read Line 1111b Memory Write and Invalidate All command encodings not shown are reserved. The ICH6 does not decode reserved values, and therefore will not respond if a PCI master generates a cycle using one of the reserved values.
DEVSEL#	I/O	**Device Selec**t: The ICH6 asserts DEVSEL# to claim a PCI transaction. As an output, the ICH6 asserts DEVSEL# when a PCI master peripheral attempts an access to an internal ICH6 address or an address destined DMI (main memory or graphics). As an input, DEVSEL# indicates the response to an ICH6-initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PLTRST#. DEVSEL# remains tri-stated by the ICH6 until driven by a target device.
FRAME#	I/O	**Cycle Frame:** The current initiator drives FRAME# to indicate the beginning and duration of a PCI transaction. While the initiator asserts FRAME#, data transfers continue. When the initiator negates FRAME#, the transaction is in the final data phase. FRAME# is an input to the ICH6 when the ICH6 is the target, and FRAME# is an output from the ICH6 when the ICH6 is the initiator. FRAME# remains tri-stated by the ICH6 until driven by an initiator.

PCI Interface Signals (Continued)

Name	Type	Description
IRDY#	I/O	**Initiator Read**y: IRDY# indicates the ICH6's ability, as an initiator, to complete the current data phase of the transaction. It is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates the ICH6 has valid data present on AD[31:0]. During a read, it indicates the ICH6 is prepared to latch data. IRDY# is an input to the ICH6 when the ICH6 is the target and an output from the ICH6 when the ICH6 is an initiator. IRDY# remains tri-stated by the ICH6 until driven by an initiator.
TRDY#	I/O	**Target Read**y: TRDY# indicates the ICH6's ability as a target to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed when both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that the ICH6, as a target, has placed valid data on AD[31:0]. During a write, TRDY# indicates the ICH6, as a target is prepared to latch data. TRDY# is an input to the ICH6 when the ICH6 is the initiator and an output from the ICH6 when the ICH6 is a target. TRDY# is tri-stated from the leading edge of PLTRST#. TRDY# remains tri-stated by the ICH6 until driven by a target.
STOP#	I/O	**Sto**p: STOP# indicates that the ICH6, as a target, is requesting the initiator to stop the current transaction. STOP# causes the ICH6, as an initiator, to stop the current transaction. STOP# is an output when the ICH6 is a target and an input when the ICH6 is an initiator.
PAR	I/O	**Calculated/Checked Parity:** PAR uses “even” parity calculated on 36 bits, AD[31:0] plus C/BE[3:0]#. “Even” parity means that the ICH6 counts the number of one within the 36 bits plus PAR and the sum is always even. The ICH6 always calculates PAR on 36 bits regardless of the valid byte enables. The ICH6 generates PAR for address and data phases and only guarantees PAR to be valid one PCI clock after the corresponding address or data phase. The ICH6 drives and tri-states PAR identically to the AD[31:0] lines except that the ICH6 delays PAR by exactly one PCI clock. PAR is an output during the address phase (delayed one clock) for all ICH6 initiated transactions. PAR is an output during the data phase (delayed one clock) when the ICH6 is the initiator of a PCI write transaction, and when it is the target of a read transaction. ICH6 checks parity when it is the target of a PCI write transaction. If a parity error is detected, the ICH6 will set the appropriate internal status bits, and has the option to generate an NMI# or SMI#.

5.2 Intel ICH6-M South Bridge(2)

PCI Interface Signals (Continued)

Name	Type	Description
PERR#	I/O	**Parity Error**: An external PCI device drives PERR# when it receives data that has a parity error. The ICH6 drives PERR# when it detects a parity error. The ICH6 can either generate an NMI# or SMI# upon detecting a parity error (either detected internally or reported via the PERR# signal).
REQ[0:3]# **REQ[4]#** / GPI[40] **REQ[5]#** / GPI[1] **REQ[6]#** / GPI[0]	I	**PCI Request**s: The ICH6 supports up to 7 masters on the PCI bus. The REQ[4]#, REQ[5]#, and REQ[6]# pins can instead be used as a GPI.
GNT[0:3]# **GNT[4]#** / GPO[48] **GNT[5]#** / GPO[17]# **GNT[6]#** / GPO[16]#	O	**PCI Grant**s: The ICH6 supports up to 7 masters on the PCI bus. The GNT[4]# pin can instead be used as a GPO. Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail. GNT[5]#/GPO[17] and GNT[6]#/GPO[17] both have an internal pull-up. **NOTE:** GNT[6] is sampled at the rising edge of PWROK as a functional strap. See Section 2.22.1 for more details. There is a weak, integrated pull-up resistor on the GNT[6] pin.
PCICLK	I	**PCI Clock**: This is a 33 MHz clock. PCICLK provides timing for all transactions on the PCI Bus.
PCIRST#	O	**PCI Reset:** This is the Secondary PCI Bus reset signal. It is a logical OR of the primary interface PLTRST# signal and the state of the Secondary Bus Reset bit of the Bridge Control register (D30:F0:3Eh, bit 6). **NOTE:** PCIRST# is in the VccSus3_3 well.
PLOCK#	I/O	**PCI Lock**: This signal indicates an exclusive bus operation and may require multiple transactions to complete. ICH6 asserts PLOCK# when it performs non-exclusive transactions on the PCI bus. PLOCK# is ignored when PCI masters are granted the bus.
SERR#	OD I/O	**System Error**: SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the ICH6 has the ability to generate an NMI, SMI#, or interrupt.
PME#	OD I	**PCI Power Management Event**: PCI peripherals drive PME# to wake the system from low-power states S1–S5. PME# assertion can also be enabled to generate an SCI from the S0 state. In some cases the ICH6 may drive PME# active due to an internal wake event. The ICH6 will not drive PME# high, but it will be pulled up to VccSus3_3 by an internal pull-up resistor.

Serial ATA Interface Signals

Name	Type	Description
SATA[0]TXP **SATA[0]TXN**	O	**Serial ATA 0 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 0.
SATA[0]RXP **SATA[0]RXN**	I	**Serial ATA 0 Differential Receive Pair:** These are inbound high-speed differential signals from Port 0.
SATA[1]TXP **SATA[1]TXN**	O	**Serial ATA 1 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 1.
SATA[1]RXP **SATA[1]RXN**	I	**Serial ATA 1 Differential Receive Pair:** These are inbound high-speed differential signals from Port 1.
SATA[2]TXP **SATA[2]TXN**	O	**Serial ATA 2 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 2.
SATA[2]RXP **SATA[2]RXN**	I	**Serial ATA 2 Differential Receive Pair:** These are inbound high-speed differential signals from Port 2.
SATA[3]TXP **SATA[3]TXN**	O	**Serial ATA 3 Differential Transmit Pair:** These are outbound high-speed differential signals to Port 3.
SATA[3]RXP **SATA[3]RXN**	I	**Serial ATA 3 Differential Receive Pair:** These are inbound high-speed differential signals from Port 3.
SATARBIAS	O	**Serial ATA Resistor Bias:** These are analog connection points for an external resistor to ground.
SATARBIAS#	I	**Serial ATA Resistor Bias Complement:** These are analog connection points for an external resistor to ground.
SATA[0]GP / GPI[26]	I	**Serial ATA 0 General Purpose:** This is an input pin which can be configured as an interlock switch corresponding to SATA Port 0. When used as an interlock switch status indication, this signal should be drive to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. If interlock switches are not required, this pin can be configured as GPI[26]. **NOTE:** All SATAxGP pins must be configured with the same function: as either SATAxGP pins or GPI pins.
SATA[1]GP / GPI[29]	I	**Serial ATA 1 General Purpose:** Same function as SATA[0]GP, except for SATA Port 1. If interlock switches are not required, this pin can be configured as GPI[29].
SATA[2]GP / GPI[30]	I	**Serial ATA 2 General Purpose:** Same function as SATA[0]GP, except for SATA Port 2. If interlock switches are not required, this pin can be configured as GPI[30].

5.2 Intel ICH6-M South Bridge(3)

Serial ATA Interface Signals (Continued)

Name	Type	Description
SATA[3]GP / GPI[31]	I	**Serial ATA 3 General Purpose:** Same function as SATA[0]GP, except for SATA Port 3. If interlock switches are not required, this pin can be configured as GPI[31].
SATALED#	OC O	**Serial ATA LED:** This is an open-collector output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required. **NOTE:** An internal pull-up is enabled only during PLTRST# assertion.

Interrupt Signals

Name	Type	Description
SERIRQ	I/O	**Serial Interrupt Request:** This pin implements the serial interrupt protocol.
PIRQ[D:A]#	OD I	**PCI Interrupt Requests:** In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQA# is connected to IRQ16, PIRQB# to IRQ17, PIRQC# to IRQ18, and PIRQD# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]# / GPI[5:2]	OD I	**PCI Interrupt Requests:** In non-APIC mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the *Interrupt Steering* section. Each PIRQx# line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQE# is connected to IRQ20, PIRQF# to IRQ21, PIRQG# to IRQ22, and PIRQH# to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPI.
IDEIRQ	I	**IDE Interrupt Request:** This interrupt input is connected to the IDE drive.

LAN Connect Interface Signals

Name	Type	Description
LAN_CLK	I	**LAN I/F Clock:** This signal is driven by the LAN Connect component. The frequency range is 5 MHz to 50 MHz.
LAN_RXD[2:0]	I	**Received Data:** The LAN Connect component uses these signals to transfer data and control information to the integrated LAN controller. These signals have integrated weak pull-up resistors.
LAN_TXD[2:0]	O	**Transmit Data**: The integrated LAN controller uses these signals to transfer data and control information to the LAN Connect component.
LAN_RSTSYNC	O	**LAN Reset/Sync:** The LAN Connect component's Reset and Sync signals are multiplexed onto this pin.

Other Clocks

Name	Type	Description
CLK14	I	**Oscillator Clock:** This clock is used for 8254 timers. It runs at 14.31818 MHz. This clock is permitted to stop during S3 (or lower) states.
CLK48	I	**48 MHz Clock:** This clock is used to run the USB controller. IT runs at 48.000 MHz. This clock is permitted to stop during S3 (or lower) states.
SATA_CLKP SATA_CLKN	I	**100 MHz Differential Clock:** These signals are used to run the SATA controller. Runs at 100 MHz. This clock is permitted to stop during S3 (or lower) states.
DMI_CLKP, DMI_CLKN	I	**100 MHz Differential Clock:** These signals are used to run the Direct Media Interface. Runs at 100 MHz.

LPC Interface Signals

Name	Type	Description
LAD[3:0] / FWH[3:0]	I/O	**LPC Multiplexed Command, Address, Data:** For LAD[3:0], internal pull-ups are provided.
LFRAME# / FWH[4]	O	**LPC Frame:** LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ[0]# LDRQ[1]# / GPI[41]	I	**LPC Serial DMA/Master Request Inputs:** LDRQ[1:0]# are used to request DMA or bus master access. These signals are typically connected to external Super I/O device. An internal pull-up resistor is provided on these signals. LDRQ[1]# may optionally be used as GPI.

5.2 Intel ICH6-M South Bridge(4)

IDE Interface Signals

Name	Type	Description
DCS1#	O	**IDE Device Chip Selects for 100 Range:** For ATA command register block. This output signal is connected to the corresponding signal on the IDE connector.
DCS3#	O	**IDE Device Chip Select for 300 Range:** For ATA control register block. This output signal is connected to the corresponding signal on the IDE connector.
DA[2:0]	O	**IDE Device Address:** These output signals are connected to the corresponding signals on the IDE connector. They are used to indicate which byte in either the ATA command block or control block is being addressed.
DD[15:0]	I/O	**IDE Device Data:** These signals directly drive the corresponding signals on the IDE connector. There is a weak internal pull-down resistor on DD7.
DDREQ	I	**IDE Device DMA Request:** This input signal is directly driven from the DRQ signal on the IDE connector. It is asserted by the IDE device to request a data transfer, and used in conjunction with the PCI bus master IDE function and are not associated with any AT compatible DMA channel. There is a weak internal pull-down resistor on this signal.
DDACK#	O	**IDE Device DMA Acknowledge:** This signal directly drives the DAK# signal on the IDE connector. DDACK# is asserted by the Intel ICH6 to indicate to IDE DMA slave devices that a given data transfer cycle (assertion of DIOR# or DIOW#) is a DMA data transfer cycle. This signal is used in conjunction with the PCI bus master IDE function and are not associated with any AT-compatible DMA channel.
DIOR# / (DWSTB / RDMARDY#)	O	**DIOR# /** **Disk I/O Read (PIO and Non-Ultra DMA)**: This is the command to the IDE device that it may drive data onto the DD lines. Data is latched by the ICH6 on the de-assertion edge of DIOR#. The IDE device is selected either by the ATA register file chip selects (DCS1# or DCS3#) and the DA lines, or the IDE DMA acknowledge (DDAK#) Disk Write Strobe (Ultra DMA Writes to Disk): This is the data write strobe for writes to disk. When writing to disk, ICH6 drives valid data on rising and falling edges of DWSTB. Disk DMA Ready (Ultra DMA Reads from Disk): This is the DMA ready for reads from disk. When reading from disk, ICH6 de-asserts RDMARDY# to pause burst data transfers.

IDE Interface Signals (Continued)

Name	Type	Description
DIOW# / (DSTOP)	O	**Disk I/O Write (PIO and Non-Ultra DMA)**: This is the command to the IDE device that it may latch data from the DD lines. Data is latched by the IDE device on the de-assertion edge of DIOW#. The IDE device is selected either by the ATA register file chip selects (DCS1# or DCS3#) and the DA lines, or the IDE DMA acknowledge (DDAK#). Disk Stop (Ultra DMA): ICH6 asserts this signal to terminate a burst.
IORDY / (DRSTB / WDMARDY#)	I	**I/O Channel Ready (PIO)**: This signal will keep the strobe active (DIOR# on reads, DIOW# on writes) longer than the minimum width. It adds wait-states to PIO transfers. Disk Read Strobe (Ultra DMA Reads from Disk): When reading from disk, ICH6 latches data on rising and falling edges of this signal from the disk. Disk DMA Ready (Ultra DMA Writes to Disk): When writing to disk, this is de-asserted by the disk to pause burst data transfers.

System Management Interface Signals

Name	Type	Description
INTRUDER#	I	**Intruder Detect:** This signal can be set to disable system if box detected open. This signal's status is readable, so it can be used like a GPI if the Intruder Detection is not needed.
SMLINK[1:0]	OD I/O	**System Management Link:** SMBus link to optional external system management ASIC or LAN controller. External pull-ups are required. Note that SMLINK0 corresponds to an SMBus Clock signal, and SMLINK1 corresponds to an SMBus Data signal.
LINKALERT#	OD I/O	**SMLink Alert:** Output of the integrated LAN and input to either the integrated ASF or an external management controller in order for the LAN's SMLINK slave to be serviced.

SM Bus Interface Signals

Name	Type	Description
SMBDATA	OD I/O	**SMBus Data:** External pull-up resistor is required.
SMBCLK	OD I/O	**SMBus Clock:** External pull-up resistor is required.
SMBALERT#/ GPI[11]	I	**SMBus Alert:** This signal is used to wake the system or generate SMI#. If not used for SMBALERT#, it can be used as a GPI.

5.2 Intel ICH6-M South Bridge(5)

USB Interface Signals

Name	Type	Description
USBP[0]P, USBP[0]N, USBP[1]P, USBP[1]N	I/O	**Universal Serial Bus Port [1:0] Differentia**l: These differential pairs are used to transmit Data/Address/Command signals for ports 0 and 1. These ports can be routed to UHCI controller #1 or the EHCI controller. **NOTE:** No external resistors are required on these signals. The ICH6 integrates 15 KΩ pull-downs and provides an output driver impedance of 45Ω which requires no external series resistor
USBP[2]P, USBP[2]N, USBP[3]P, USBP[3]N	I/O	**Universal Serial Bus Port [3:2] Differentia**l: These differential pairs are used to transmit data/address/command signals for ports 2 and 3. These ports can be routed to UHCI controller #2 or the EHCI controller. **NOTE:** No external resistors are required on these signals. The ICH6 integrates 15 KΩ pull-downs and provides an output driver impedance of 45Ω which requires no external series resistor
USBP[4]P, USBP[4]N, USBP[5]P, USBP[5]N	I/O	**Universal Serial Bus Port [5:4] Differentia**l: These differential pairs are used to transmit Data/Address/Command signals for ports 4 and 5. These ports can be routed to UHCI controller #3 or the EHCI controller. **NOTE:** No external resistors are required on these signals. The ICH6 integrates 15 KΩ pull-downs and provides an output driver impedance of 45Ω which requires no external series resistor
USBP[6]P, USBP[6]N, USBP[7]P, USBP[7]N	I/O	**Universal Serial Bus Port [7:6] Differentia**l: These differential pairs are used to transmit Data/Address/Command signals for ports 6 and 7. These ports can be routed to UHCI controller #4 or the EHCI controller. **NOTE:** No external resistors are required on these signals. The ICH6 integrates 15 KΩ pull-downs and provides an output driver impedance of 45Ω which requires no external series resistor
OC[3:0]# **OC[4]#** / GPI[9] **OC[5]#** / GPI[10] **OC[6]#** / GPI[14] **OC[7]#** / GPI[15]	I	**Overcurrent Indicator**s: These signals set corresponding bits in the USB controllers to indicate that an overcurrent condition has occurred. OC[7:4]# may optionally be used as GPIs. **NOTE:** OC[7:0]# are not 5 V tolerant.
USBRBIAS	O	**USB Resistor Bias:** Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.
USBRBIAS#	I	**USB Resistor Bias Complement:** Analog connection point for an external resistor. Used to set transmit currents and internal load resistors.

EEPROM Interface Signals

Name	Type	Description
EE_SHCLK	O	**EEPROM Shift Cloc**k: This signal is the serial shift clock output to the EEPROM.
EE_DIN	I	**EEPROM Data I**n: This signal transfers data from the EEPROM to the Intel ® ICH6. This signal has an integrated pull-up resistor.
EE_DOUT	O	**EEPROM Data Ou**t: This signal transfers data from the ICH6 to the EEPROM.
EE_CS	O	**EEPROM Chip Selec**t: This is the chip select signal to the EEPROM.

Miscellaneous Signals

Name	Type	Description
INTVRMEN	I	**Internal Voltage Regulator Enable:** This signal enables the internal 1.5 V Suspend regulator when connected to VccRTC. When connected to Vss, the internal regulator is disabled
SPKR	O	**Speaker:** The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device that in turn drives the system speaker. Upon PLTRST#, its output state is 0. **NOTE:** SPKR is sampled at the rising edge of PWROK as a functional strap. See Section 2.22.1 for more details. There is a weak integrated pull-down resistor on SPKR pin.
RTCRST#	I	**RTC Reset:** When asserted, this signal resets register bits in the RTC well. **NOTES:** 1. Unless CMOS is being cleared (only to be done in the G3 power state), the RTCRST# input must always be high when all other RTC power planes are on. **2.** In the case where the RTC battery is dead or missing on the platform, the RTCRST# pin must rise before the RSMRST# pin.
TP[0]	I	**Test Point 0:** This signal must have an external pull-up to VccSus3_3.
TP[1]	O	**Test Point 1:** Route signal to a test point.
TP[2]	O	**Test Point 2:** Route signal to a test point.
TP[3]	I	**Test Point 3:** Route signal to a test point.
TP[4]	O	**Test Point 4:** Route signal to a test point.

5.2 Intel ICH6-M South Bridge(6)

Power Management Interface Signals

Name	Type	Description
PWRBTN#	I	**Power Button:** The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S1-S4 states. This signal has an internal pull-up resistor and has an internal 16 ms de-bounce on the input.
RI#	I	**Ring Indicate:** This signal is an input from a modem. It can be enabled as a wake event, and this is preserved across power failures.
SYS_RESET#	I	**System Rese**t: This pin forces an internal reset after being debounced. The ICH6 will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms ± 2 ms for the SMBus to idle before forcing a reset on the system.
RSMRST#	I	**Resume Well Reset:** This signal is used for resetting the resume power plane logic.
LAN_RST#	I	**LAN Reset:** When asserted, the internal LAN controller will be put into reset. This signal must be asserted for at least 10 ms after the resume well power (VccSus3_3 and VccSus1_5) is valid. When de-asserted, this signal is an indication that the resume well power is stable. **NOTE:** LAN_RST# must de-assert at some point to complete ICH6 power up sequencing.
WAKE#	I	**PCI Express* Wake Event:** Sideband wake signal on PCI Express asserted by components requesting wakeup.
MCH_SYNC#	I	**MCH SYNC:** This input is internally ANDed with the PWROK input. Connected to the ICH_SYNC# output of (G)MCH.
SUS_STAT# / LPCPD#	O	**Suspend Status:** This signal is asserted by the ICH6 to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This signal is called LPCPD# on the LPC I/F.
SUSCLK	O	**Suspend Clock:** This clock is an output of the RTC generator circuit to use by other chips for refresh clock.
VRMPWRGD	I	**VRM Power Good:** This should be connected to be the processor's VRM Power Good signifying the VRM is stable. This signal is internally ANDed with the PWROK input.

Power Management Interface Signals (Continued)

Name	Type	Description
PLTRST#	O	**Platform Reset:** The ICH6 asserts PLTRST# to reset devices on the platform (e.g., SIO, FWH, LAN, (G)MCH, IDE, TPM, etc.). The ICH6 asserts PLTRST# during power-up and when S/W initiates a hard reset sequence through the Reset Control register (I/O Register CF9h). The ICH6 drives PLTRST# inactive a minimum of 1 ms after both PWROK and VRMPWRGD are driven high. The ICH6 drives PLTRST# active a minimum of 1 ms when initiated through the Reset Control register (I/O Register CF9h). **NOTE:** PLTRST# is in the VccSus3_3 well.
THRM#	I	**Thermal Alarm:** This is an active low signal generated by external hardware to generate an SMI# or SCI.
THRMTRIP#	I	**Thermal Trip**: When low, this signal indicates that a thermal trip from the processor occurred, and the ICH6 will immediately transition to a S5 state. The ICH6 will not wait for the processor stop grant cycle since the processor has overheated.
SLP_S3#	O	**S3 Sleep Control:** SLP_S3# is for power plane control. This signal shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states.
SLP_S4#	O	**S4 Sleep Control**: SLP_S4# is for power plane control. This signal shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state. **NOTE:** This pin must be used to control the DRAM power in order to use the ICH6's DRAM power-cycling feature. Refer to Chapter 5.14.10.2 for details.
SLP_S5#	O	**S5 Sleep Control:** SLP_S5# is for power plane control. This signal is used to shut power off to all non-critical systems when in the S5 (Soft Off) states.
PWROK	I	**Power OK:** When asserted, PWROK is an indication to the ICH6 that core power has been stable for at least 99 ms and PCICLK has been stable for at least 1 mS. An exception to this rule is if the system is in S3 HOT , in which PWROK may or may notstay asserted even though PCICLK may be inactive. PWROK can be driven asynchronously. When PWROK is negated, the ICH6 asserts PLTRST#. **NOTE:** PWROK must de-assert for a minimum of three RTC clock periods in order for the ICH6 to fully reset the power and properly generate the PLTRST# output

5.2 Intel ICH6-M South Bridge(7)

Processor Interface Signals

Name	Type	Description
A20M#	O	**Mask A20:** A20M# will go active based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active.
CPUSLP#	O	**Processor Sleep:** This signal puts the processor into a state that saves substantial power compared to Stop-Grant state. However, during that time, no snoops occur. The Intel® ICH6 can optionally assert the CPUSLP# signal when going to the S1 state, and will always assert it when going to C3 or C4.
FERR#	I	**Numeric Coprocessor Error:** This signal is tied to the coprocessor error signal on the processor. FERR# is only used if the ICH6 coprocessor error reporting function is enabled in the OIC.CEN register (Chipset ConfigurationRegisters:Offset 31FFh: bit 1). If FERR# is asserted, the ICH6 generates an internal IRQ13 to its interrupt controller unit. It is also used to gate the IGNNE# signal to ensure that IGNNE# is not asserted to the processor unless FERR# is active. FERR# requires an external weak pull-up to ensure a high level when the coprocessor error function is disabled. **NOTE:** FERR# can be used in some states for notification by the processor of pending interrupt events. This functionality is independent of the OIC register bit setting.
IGNNE#	O	**Ignore Numeric Error:** This signal is connected to the ignore error pin on the processor. IGNNE# is only used if the ICH6 coprocessor error reporting function is enabled in the OIC.CEN register (Chipset Configuration Registers:Offset 31FFh: bit 1). If FERR# is active, indicating a coprocessor error, a write to the Coprocessor Error register (I/O register F0h) causes the IGNNE# to be asserted. IGNNE# remains asserted until FERR# is negated. If FERR# is not asserted when the Coprocessor Error register is written, the IGNNE# signal is not asserted.
INIT#	O	**Initialization:** INIT# is asserted by the ICH6 for 16 PCI clocks to reset the processor. ICH6 can be configured to support processor Built In Self Test (BIST).
INIT3_3V#	O	**Initialization 3.3 V:** This is the identical 3.3 V copy of INIT# intended for Firmware Hub.
INTR	O	**Processor Interrupt:** INTR is asserted by the ICH6 to signal the processor that an interrupt request is pending and needs to be serviced. It is an asynchronous output and normally driven low.

Processor Interface Signals (Continued)

Name	Type	Description
NMI	O	**Non-Maskable Interrupt:** NMI is used to force a non-Maskable interrupt to the processor. The ICH6 can generate an NMI when either SERR# is asserted or IOCHK# goes active via the SERIRQ# stream. The processor detects an NMI when it detects a rising edge on NMI. NMI is reset by setting the corresponding NMI source enable/disable bit in the NMI Status and Control register (I/O Register 61h).
SMI#	O	**System Management Interrupt:** SMI# is an active low output synchronous to PCICLK. It is asserted by the ICH6 in response to one of many enabled hardware or software events.
STPCLK#	O	**Stop Clock Request:** STPCLK# is an active low output synchronous to PCICLK. It is asserted by the ICH6 in response to one of many hardware or software events. When the processor samples STPCLK# asserted, it responds by stopping its internal clock.
RCIN#	I	**Keyboard Controller Reset CPU:** The keyboard controller can generate INIT# to the processor. This saves the external OR gate with the ICH6's other sources of INIT#. When the ICH6 detects the assertion of this signal, INIT# is generated for 16 PCI clocks. **NOTE:** The ICH6 will ignore RCIN# assertion during transitions to the S1, S3, S4, and S5 states.
A20GATE	I	**A20 Gate:** A20GATE is from the keyboard controller. The signal acts as an alternative method to force the A20M# signal active. It saves the external OR gate needed with various other chipsets.
CPUPWRGD / GPO[49]	OD O	**Processor Power Good:** This signal should be connected to the processor's PWRGOOD input to indicate when the processor power is valid. This is an open- drain output signal (external pull-up resistor required) that represents a logical AND of the ICH6's PWROK and VRMPWRGD signals. This signal may optionally be configured as a GPO.

5.2 Intel ICH6-M South Bridge(8)

General Purpose I/O Signals 1,2

Name	Type	Tolerance	Power Well	Description
GPO[49]	OD O	V_CPU_IO	`Core	This signal is fixed as output only and can instead be used as CPUPWRGD.
GPO[48]	O	3.3 V	Core	This signal is fixed as output only and can instead be used as GNT4#.
GPIO[47:42]	N/A	N/A	N/A	This signal is not implemented.
GPI[41]	I	3.3 V	Core	This signal is fixed as input only and can be used instead as LDRQ1#.
GPI[40]	I	5 V	Core	This signal is fixed as input only and can be used instead as REQ4#.
GPIO[39:35]	N/A	N/A	N/A	This signal is not implemented.
GPIO[34:33]	I/O	3.3 V	Core	This signal can be input or output and is unmultiplexed
GPIO[32]	I/O	3.3 V	Core	This signal can be input or output.
GPI[31]	I	3.3 V	Core	This signal is fixed as input only and can instead be used for SATA[3]GP.
GPI[30]	I	3.3 V	Core	This signal is fixed as input only and can instead be used for SATA[2]GP.
GPI[29]	I	3.3 V	Core	This signal is fixed as input only and can instead be used for SATA[1]GP.
GPIO[28:27]	I/O	3.3 V	Resume	This signal can be input or output and is unmultiplexed.
GPI[26]	I	3.3 V	Core	This signal is fixed as input only and can instead be used for SATA[0]GP.
GPIO[25]	I/O	3.3 V	Resume	This signal can be input or output and is unmultiplexed. It is a strap for internal Vcc2_5 regulator. See Section 2.22.1.
GPIO[24]	I/O	3.3 V	Resume	This signal can be input or output and is unmultiplexed.
GPO[23]	O	3.3 V	Core	This signal is fixed as output only.
GPIO[22]	N/A	N/A	N/A	This signal is not Implemented
GPO[21]	O	3.3 V	Core	This signal is fixed as output only and is unmultiplexed
GPO[20]	O	3.3 V	Core	This signal is fixed as output only.
GPO[19]	O	3.3 V	Core	This signal is fixed as output only. **NOTE:** GPO[19] may be programmed to blink (controllable by GPO_BLINK (D31:F0:Offset GPIOBASE+18h:bit 19)).

General Purpose I/O Signals 1,2 (Continued)

Name	Type	Tolerance	Power Well	Description
GPO[18]	O	3.3 V	Core	This signal is fixed as output only. **NOTE:** GPO[18] will blink by default immediately after reset (controllable by GPO_BLINK (D31:F0:Offset GPIOBASE+18h:bit 18)).
GPO[17]	O	3.3 V	Core	This signal is fixed as output only and can be used instead as PCI GNT[5]#.
GPO[16]	O	3.3 V	Core	This signal is fixed as output only and can be used instead as PCI GNT[6]#.
GPI[15:14]3	I	3.3 V	Resume	This signal is fixed as input only and can be used instead as OC[7:6]#
GPI[13]3	I	3.3 V	Resume	This signal is fixed as input only and is unmultiplexed.
GPI[12]3	I	3.3 V	Core	This signal is fixed as input only and is unmultiplexed.
GPI[11]3	I	3.3 V	Resume	This signal is fixed as input only and can be used instead as SMBALERT#.
GPI[10:9]3	I	3.3 V	Resume	This signal is fixed as input only and can be used instead as OC[5:4]#.
GPI[8]3	I	3.3 V	Resume	This signal is fixed as input only and is unmultiplexed.
GPI[7]3	I	3.3 V	Core	This signal is fixed as input only and is unmultiplexed.
GPI[6]3	I	3.3 V	Core	This signal is fixed as input only.
GPI[5:2]3	I	5 V	Core	This signal is fixed as input only and can be used instead as PIRQ[H:E]#.
GPI[1:0]3	I	5 V	Core	This signal is fixed as input only and can be used instead as PCI REQ[6:5]#.

NOTES:

1.All inputs are sticky. The status bit remains set as long as the input was asserted for two clocks.GPIs are sampled on PCI clocks in S0/S1. GPIs are sampled on RTC clocks in S3/S4/S5.

2.Some GPIOs exist in the VccSus3_3 power plane. Care must be taken to make sure GPIO signals are not driven high into powered-down planes. Some ICH6 GPIOs may be connected to pins on devices that exist in the core well. If these GPIOs are outputs, there is a danger that a loss of core power (PWROK low) or a Power Button Override event will result in the Intel ICH6 driving a pin to a logic 1 to another device that is powered down.

3.GPI[15:0] can be configured to cause a SMI# or SCI. Note that a GPI can be routed to either an SMI# or an SCI, but not both.

5.2 Intel ICH6-M South Bridge(9)

AC '97/Intel ® High Definition Audio Link Signals

Name	Type	Description
ACZ_RST#	O	**AC '97/Intel ® High Definition Audio Reset:** Master hardware reset to external codec(s).
ACZ_SYNC	O	**AC '97/Intel High Definition Audio Sync:** 48 kHz fixed rate sample sync to the codec(s). Also used to encode the stream number.
ACZ_BIT_CLK	I/O	**AC '97 Bit Clock Input:** 12.288 MHz serial data clock generated by the external codec(s). This signal has an integrated pull-down resistor (see Note below). **Intel High Definition Audio Bit Clock Output:** 24.000 MHz serial data clock generated by the Intel® High Definition Audio controller (the Intel ICH6). Thissignal has an integrated pull-down resistor so that ACZ_BIT_CLK does not float when an Intel High Definition Audio codec (or no codec) is connected but the signals are temporarily configured as AC '97.
ACZ_SDOUT	O	**AC '97/Intel High Definition Audio Serial Data Out:** Serial TDM data output to the codec(s). This serial output is double-pumped for a bit rate of 48 Mb/s for Intel High Definition Audio. **NOTE:** ACZ_SDOUT is sampled at the rising edge of PWROK as a functional strap. See Section 2.22.1 for more details. There is a weak integrated pull-down resistor on the ACZ_SDOUT pin.
ACZ_SDIN[2:0]	I	**AC '97/Intel High Definition Audio Serial Data In [2:0**]: Serial TDM data inputs from the three codecs. The serial input is single-pumped for a bit rate of 24 Mb/s for Intel High Definition Audio. These signals have integrated pull-down resistors, which are always enabled.

NOTES:

1. Some signals have integrated pull-ups or pull-downs. Consult table in Section 3.1 for details.
2. Intel High Definition Audio mode is selected through D30:F1:40h, bit 0: AZ/AC97#. This bit selects the mode of the shared Intel High Definition Audio/AC '97 signals. When set to 0 AC '97 mode is selected. When set to 1 Intel High Definition Audio mode is selected. The bit defaults to 0 (AC '97 mode).

Firmware Hub Interface Signals

Name	Type	Description
FWH[3:0] / LAD[3:0]	I/O	**Firmware Hub Signals.** These signals are multiplexed with the LPC address signals.
FWH[4] / LFRAME#	O	**Firmware Hub Signals.** This signal is multiplexed with the LPC LFRAME# signal.

Power and Ground Signals

Name	Description
Vcc3_3	3.3 V supply for core well I/O buffers (22 pins). This power may be shut off in S3, S4, S5 or G3 states.
Vcc1_5_A	1.5 V supply for core well logic, group A (52 pins). This power may be shut off in S3, S4, S5 or G3 states.
Vcc1_5_B	1.5 V supply for core well logic, group B (45 pins). This power may be shut off in S3, S4, S5 or G3 states.
Vcc2_5	2.5V supply for internal logic (2 pins). This power may be shut off in S3, S4, S5 or G3 states. **NOTE:** This voltage may be generated internally (see Section 2.22.1 for strapping option). If generated internally, these pins should not be connected to an external supply.
V5REF	Reference for 5 V tolerance on core well inputs (2 pins). This power may be shut off in S3, S4, S5 or G3 states.
VccSus3_3	3.3 V supply for resume well I/O buffers (20 pins). This power is not expected to be shut off unless the system is unplugged.
VccSus1_5	1.5 V supply for resume well logic (3 pin). This power is not expected to be shut off unless the system is unplugged. This voltage may be generated internally (see Section 2.22.1 for strapping option). If generated internally, these pins should not be connected to an external supply.
V5REF_Sus	Reference for 5 V tolerance on resume well inputs (1 pin). This power is not expected to be shut off unless the system is unplugged.
VccRTC	3.3 V (can drop to 2.0 V min. in G3 state) supply for the RTC well (1 pin). This power is not expected to be shut off unless the RTC battery is removed or completely drained. **NOTE:** Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS in an ICH6-based platform can be done by using a jumper on RTCRST# or GPI.
VccUSBPLL	1.5 V supply for core well logic (1 pin). This signal is used for the USB PLL. This power may be shut off in S3, S4, S5 or G3 states. This signal must be powered even if USB not used.
VccDMIPLL	1.5 V supply for core well logic (1 pins). This signal is used for the DMI PLL. This power may be shut off in S3, S4, S5 or G3 states.
VccSATAPLL	1.5 V supply for core well logic (1 pins). This signal is used for the SATA PLL. This power may be shut off in S3, S4, S5 or G3 states. This signal must be powered even if SATA not used.
V_CPU_IO	Powered by the same supply as the processor I/O voltage (3 pins). This supply is used to drive the processor interface signals listed in Table 2-13.
Vss	Grounds (172 pins).

5.2 Intel ICH6-M South Bridge(10)

Functional Strap Definitions 1

Signal	Usage	When Sampled	Description
GNT[6]#/ GPO[16]	Top-Block Swa Override	Rising Edge of PWROK	The signal has a weak internal pull-up. If the signal is sampled low, this indicates that the system is strapped to the “top-block swap” mode (ICH6 inverts A16 for all cycles targeting FWH BIOS space). The status of this strap is readable via the Top Swap bit (Chipset Configuration Registers:Offset 3414h:bit 0). Note that software will not be able to clear the Top-Swap bit until the system is rebooted without GNT6# being pulled down.
LINKALERT #	Reserved		This signal requires an external pull-up resistor.
SPKR	No Reboot	Rising Edge ofPWROK	The signal has a weak internal pull-down. If the signal is.sampled high, this indicates that the system is strapped to.the “No Reboot” mode (ICH6 will disable the TCO Timer. system reboot feature). The status of this strap is readable. via the NO REBOOT bit (Chipset Configuration. Registers:Offset 3410h:bit 5).
INTVRMEN	IntegratedVccSu 1_5VRM Enable/Disable	Always	This signal enables integrated VccSus1_5 VRM when.sampled high.
GPIO[25]	Integrated Vcc2_5 VRM Enable/ Disable	Rising Edge of RSMRST#	This signal enables integrated Vcc2_5 VRM when sampled low. This signal has a weak internal pull-up during RSMRST# and is disabled within 100 ms after RSMRST# de-asserts.
EE_CS	Reserved		This signal has a weak internal pull-down. **NOTE:** This signal should not be pulled high.
GNT[5]#/ GPO[17]	Boot BIOS Destination Selection	Rising Edge of PWROK	This signal has a weak internal pull-up. Allows for select memory ranges to be forwarded out the PCI Interface as opposed to the Firmware Hub. When sampled high, destination is LPC. Also controllable via Boot BIOS Destination bit (Chipset Configuration Registers:Offset 3410h:bit 3). **NOTE:** This functionality intended for debug/testing only.

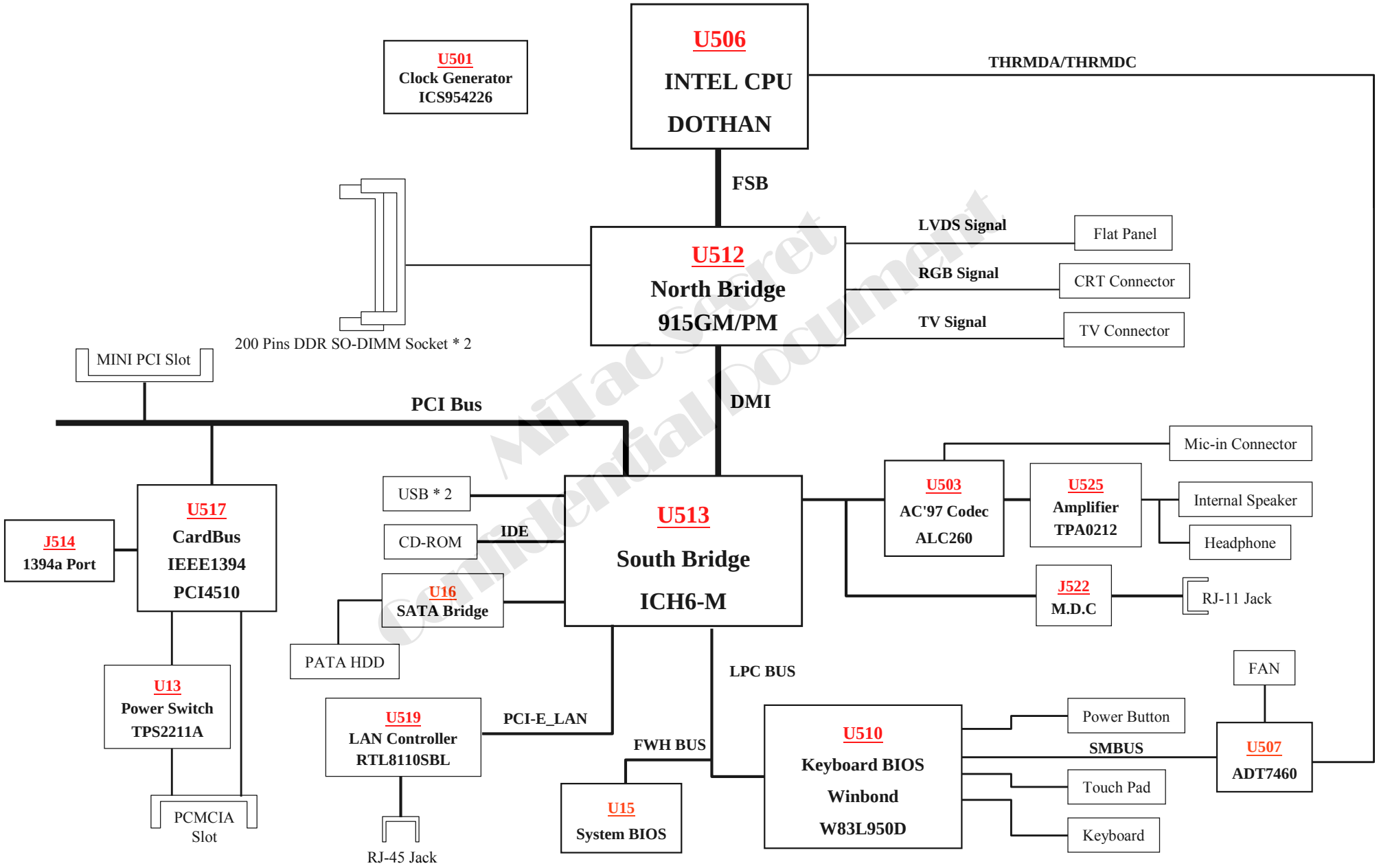
Functional Strap Definitions 1 (Continued)

Signal	Usage	When Sampled	Description
EE_DOUT	Reserved		This signal has a weak internal pull-up. **NOTE:** This signal should not be pulled low.
ACZ_SDOUT	XOR Chain Entrance / PCI Express* Port Configu-ration bit 1	Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP[3] pulled low at rising edge of PWROK. See Chapter 24 for XOR Chain functionality information. When TP[3] not pulled low at rising edge of PWROK, sets bit 1 of RPC.PC (Chipset Configuration Registers:Offset 224h). See Section 7.1.30 for details. This signal has a weak internal pull-down.
ACZ_SYNC	PCI Express Por Configu-ration bit 0	Rising Edge of PWROK	This signal has a weak internal pull-down. Sets bit 0 of RPC.PC (Chipset Configuration Registers: Off set 224h). See Section 7.1.30 for details.
TP[1]	Reserved		This signal has a weak internal pull-down. **NOTE:** This signal should not be pulled high.
SATALED#	Reserved		This signal has a weak internal pull-up enabled only when PLTRST# is asserted. **NOTE:** This signal should not be pulled low.
REQ[4:1]#	XOR Chain Selection	Rising Edge of PWROK	See Chapter 24 for functionality information.
TP[3]	XOR Chain Entrance	Rising Edge of PWROK	See Chapter 24 for functionality information. This signal has a weak internal pull-up. **NOTE:** This signal should not be pulled low unless using XOR Chain testing.

Real Time Clock Interface

Name	Type	Description
RTCX1	Special	**Crystal Input 1:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX1 can be driven with the desired clock rate.
RTCX2	Special	**Crystal Input 2:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX2 should be left floating.

6. System Block Diagram



7. Maintenance Diagnostics

7.1 Introduction

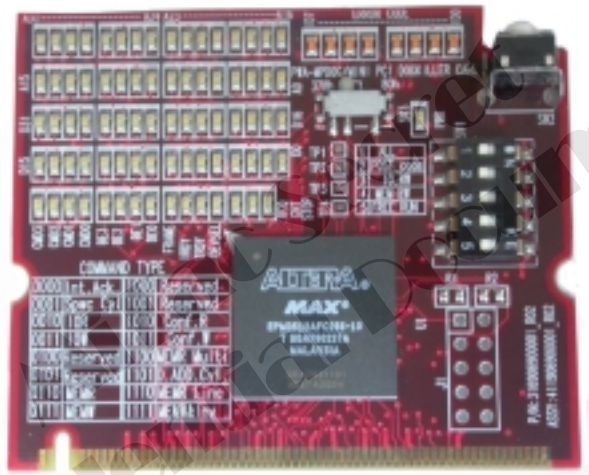
Each time the computer is turned on, the system BIOS runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized, then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to the port-80H by the debug card plug at MINI PCI slot.

7.2 Maintenance Diagnostics

7.2.1 Diagnostic Tool for Mini PCI Slot :



P/N:411906900001
Description: PWA; PWA-MPDOG/MINI PCI DOGKILLER CARD
Note: Order it from MIC/TSSC

7.3 Error Codes-1

Following is a list of error codes in sequent display on the MINI PCI debug board.

Code	POST Routine Description
10h	Some Type of Lone Reset
11h	Turn off FAST A20 for Post
12h	Signal Power On Reset
13h	Initialize the Chipset
14h	Search for ISA Bus VGA Adapter
15h	Reset Counter / Timer 1
16h	User Register Config through CMOS
17h	Size Memory
18h	Dispatch to RAM Test
19h	Check sum the ROM
1Ah	Reset PIC's
1Bh	Initialize Video Adapter(s)
1Ch	Initialize Video (6845Regs)
1Dh	Initialize Color Adapter
1Eh	Initialize Monochrome Adapter
1Fh	Test 8237A Page Registers

Code	POST Routine Description
20h	Test Keyboard
21h	Test Keyboard Controller
22h	Check if CMOS RAM valid
23h	Test Battery Fail & CMOS X-SUM
24h	Test the DMA Controller
25h	Initialize 8237A Controller
26h	Initialize Int Vectors
27h	RAM Quick Sizing
28h	Protected Mode Entered Safely
29h	RAM Test Completed
2Ah	Protected Mode Exit Successful
2Bh	Setup Shadow
2Ch	Going to Initialize Video
2Dh	Search for Monochrome Adapter
2Eh	Search for Color Adapter
2Fh	Sign on Messages Displayed

7.3 Error Codes-2

Following is a list of error codes in sequent display on the MINI PCI debug board.

Code	POST Routine Description
30h	Special Init of Keyboard Controller
31h	Test if Keyboard Present
32h	Test Keyboard Interrupt
33h	Test Keyboard Command Byte
34h	Test, Blank and Count all RAM
35h	Protected Mode Entered Safely(2)
36h	RAM Test Complete
37h	Protected Mode Exit Successful
38h	Update Output Port
39h	Setup Cache Controller
3Ah	Test if 18.2Hz Periodic Working
3Bh	Test for RTC ticking
3Ch	Initialize the Hardware Vectors
3Dh	Search and Init the Mouse
3Eh	Update NUMLOCK status
3Fh	Special Init of COMM and LPT Ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the Floppies
42h	Initialize the Hard Disk
43h	Initialize Option ROMs
44h	OEM's Init of Power Management
45h	Update NUMLOCK Status
46h	Test for Coprocessor Installed
47h	OEM functions before Boot
48h	Dispatch to Operate System Boot
49h	Jump into Bootstrap Code

8. Trouble Shooting

- 8.1 No Power(*1)
- 8.2 No Display(*2)
- 8.3 VGA Controller Failure LCD No Display
- 8.4 External Monitor No Display
- 8.5 Memory Test Error
- 8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error
- 8.7 Hard Driver Test Error
- 8.8 CD-ROM Driver Test Error
- 8.9 USB Port Test Error
- 8.10 Audio Failure
- 8.11 LAN Test Error
- 8.12 PC Card Socket Failure

*1: No Power Definition

Base on ACPI Spec. We define the no power as while we press the power button, the system can't leave S5 status or none the PG signal send out from power supply.

Judge condition:

- Check whether there are any voltage feedback control to turn off the power.
- Check whether no CPU power will cause system can't leave S5 status.

If there are not any diagram match these condition, we should stop analyzing the schematic in power supply sending out the PG signal. If yes, we should add the effected analysis into no power chapter.

*2: No Display Definition

Base on the digital IC three basic working conditions: working power, reset, Clock. We define the no display as while system leave S5 status but can't get into S0 status.

Judge condition:

- Check which power will cause no display.
- Check which reset signal will cause no display.
- Check which Clock signal will cause no display

Base on these three conditions to analyze the schematic and edit the no display chapter.

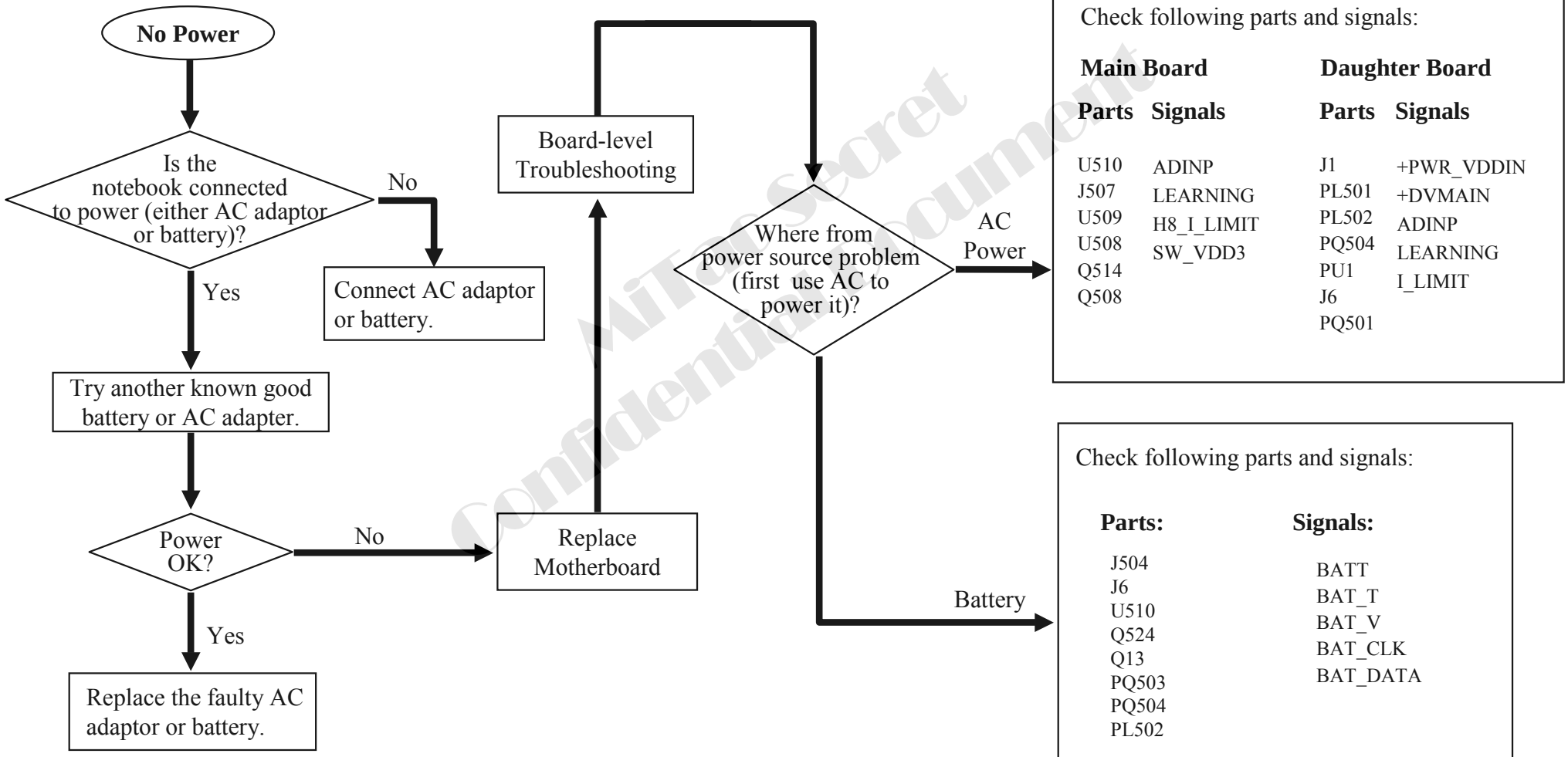
Keyword:

- S5: *Soft Off*
- S0: *Working*

For detail please refer the ACPI specification

8.1 No Power-1

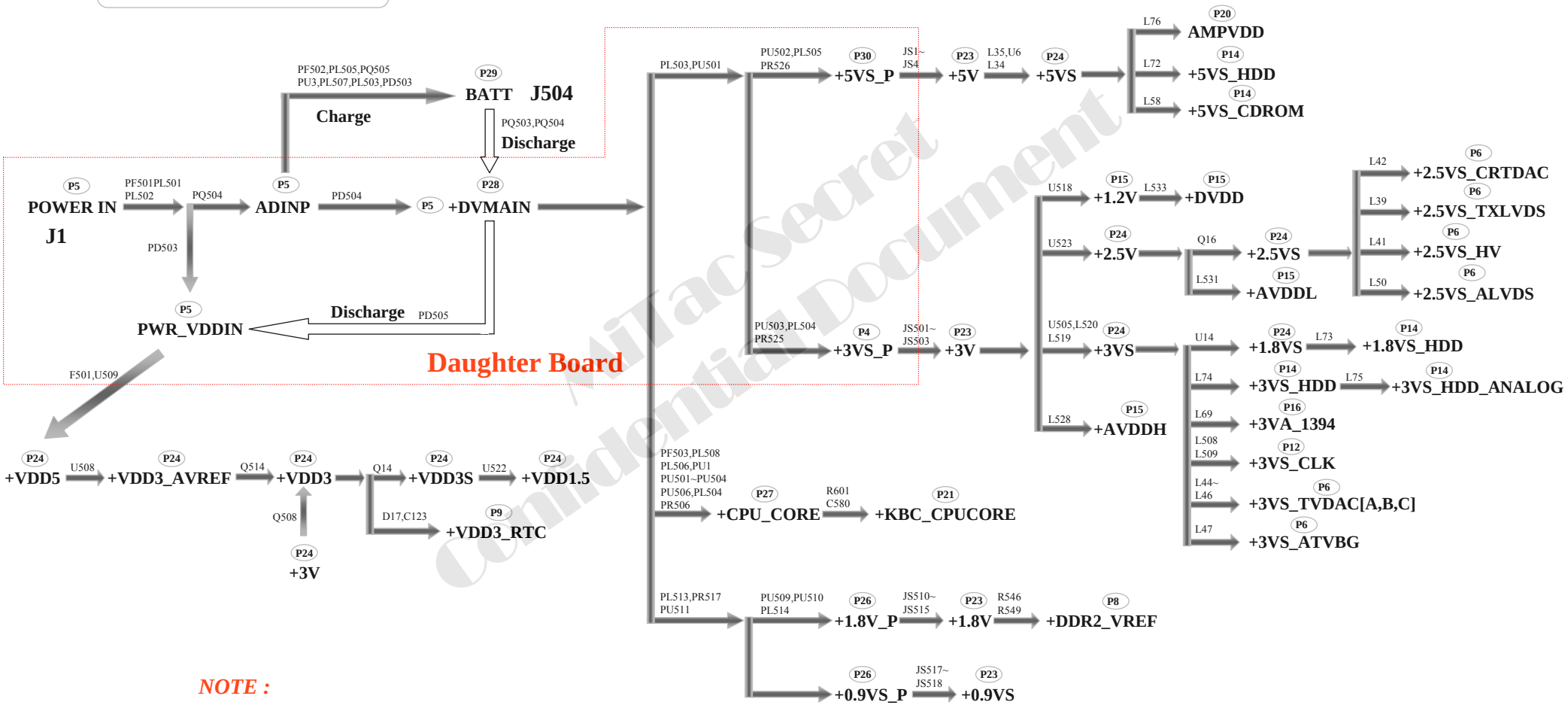
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8.1 No Power-2

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Main Voltage Map



NOTE :

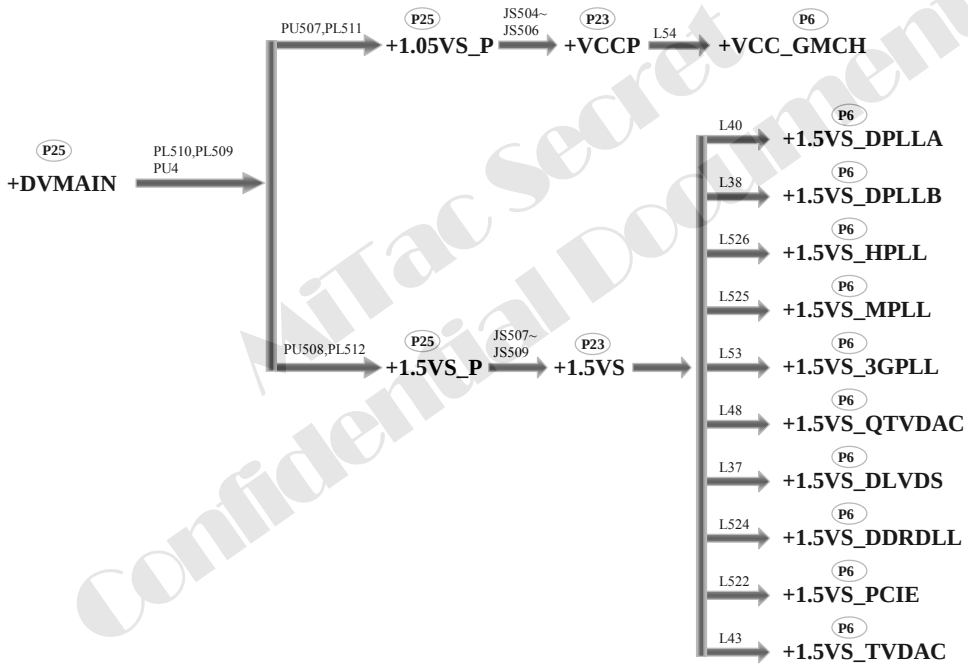
P2 : Page 2 on M/B or Daughter Board circuit diagram.

PF501 : Through by part PF501.

8.1 No Power-3

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Main Voltage Map



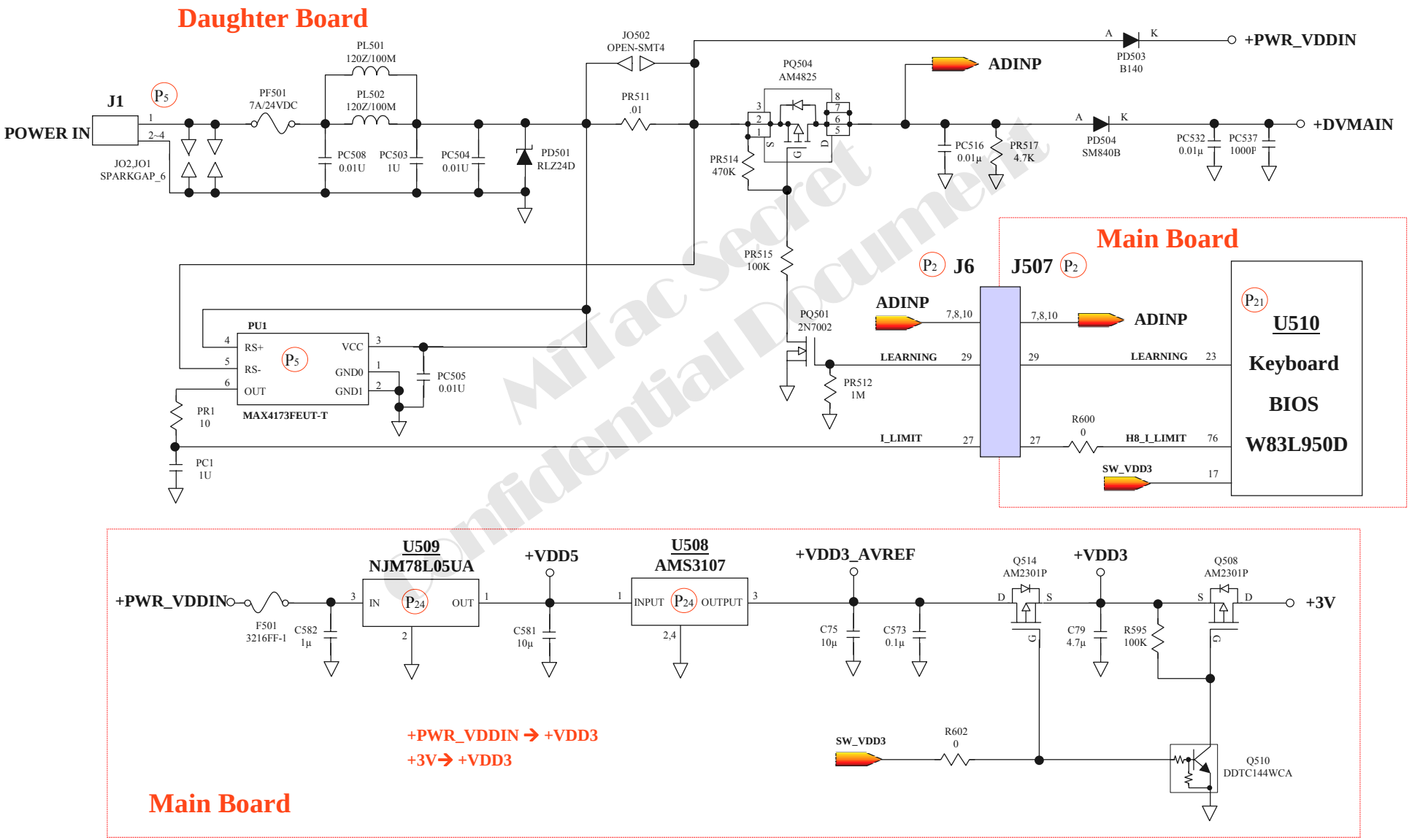
NOTE :

P25 : Page 25 on M/B Board circuit diagram.

PL510 : Through by part PL510.

8.1 No Power-4

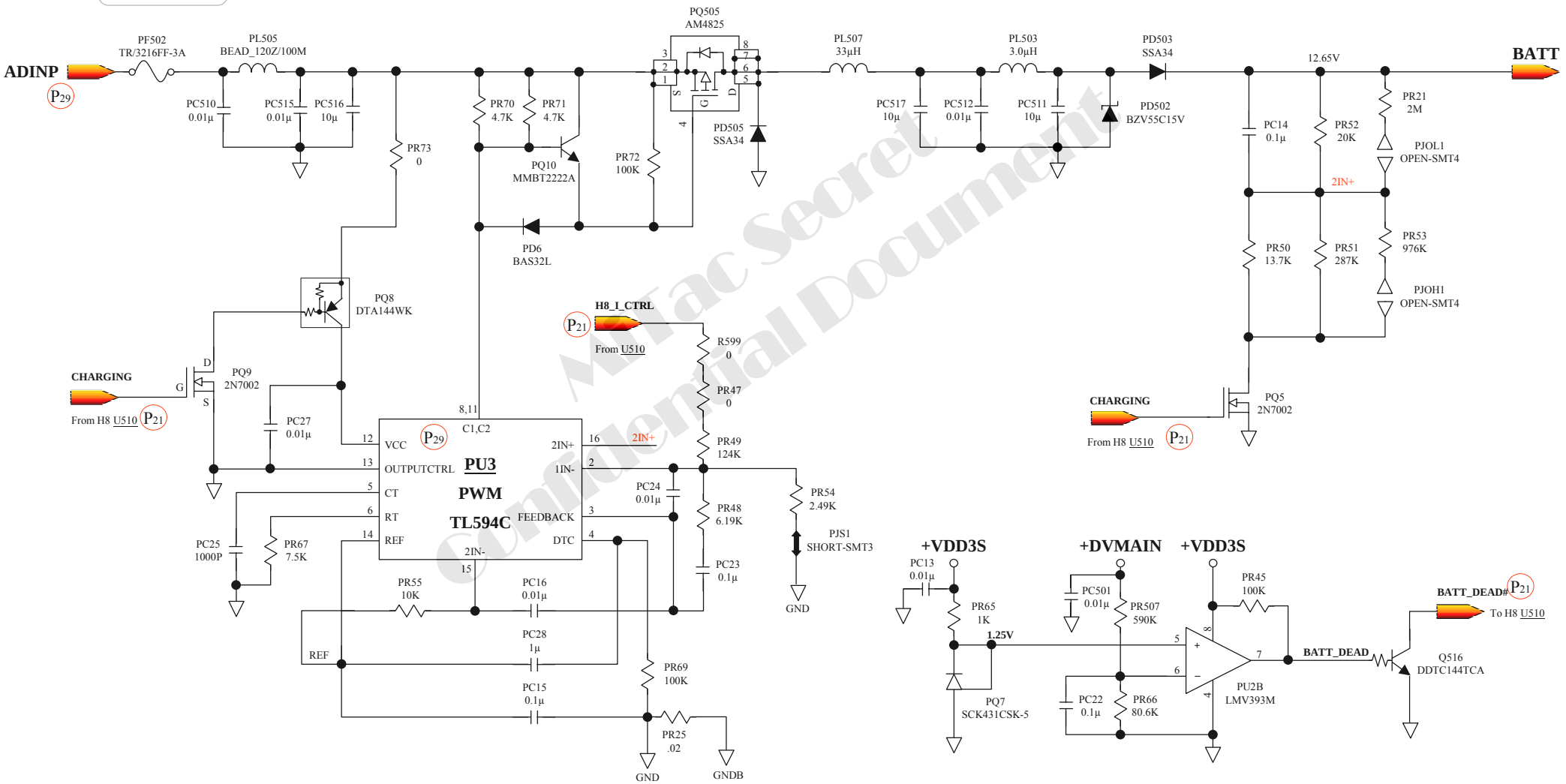
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.



8.1 No Power-5

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

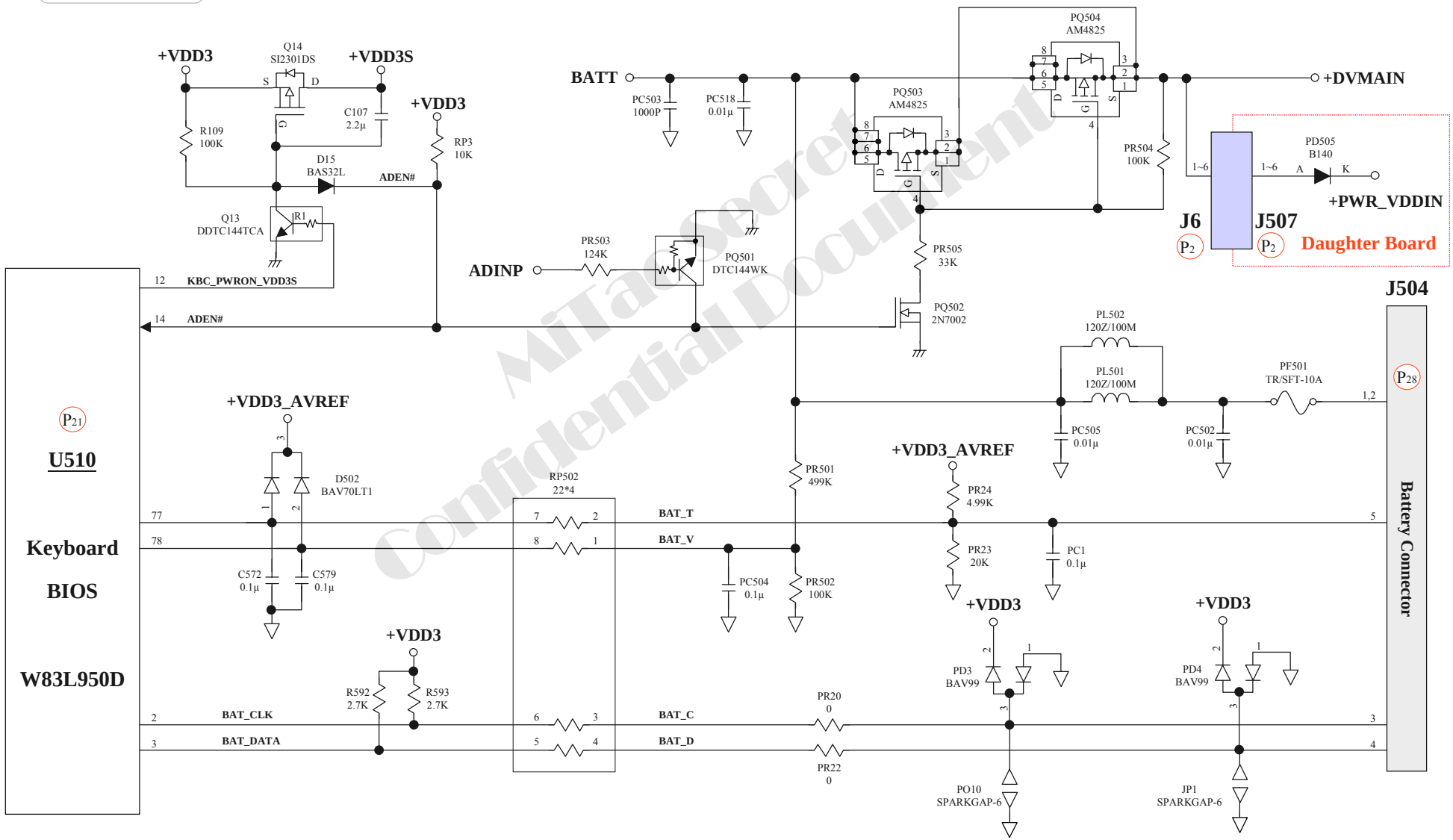
Charge



8.1 No Power-6

When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

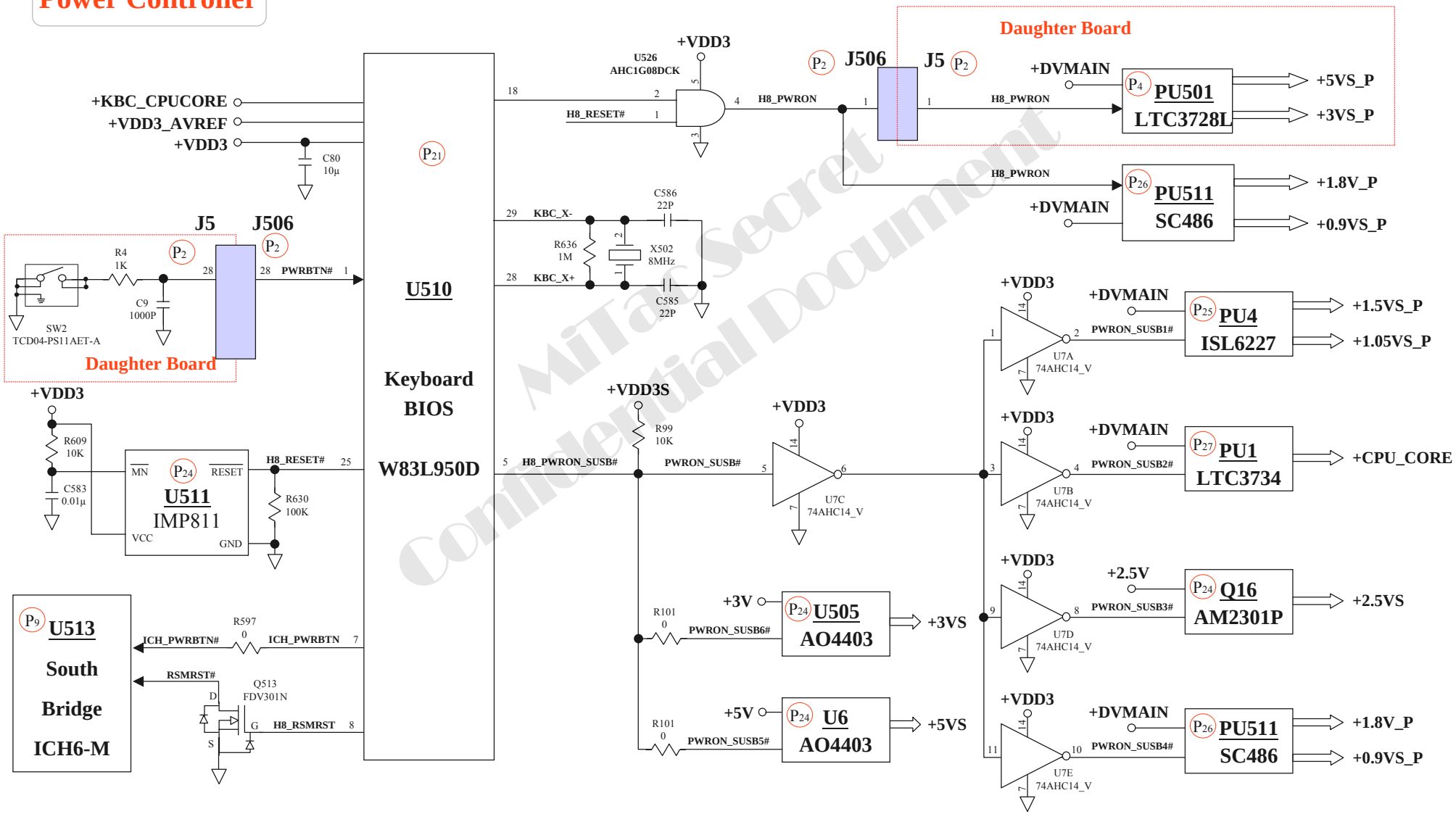
Discharge



8.1 No Power-7

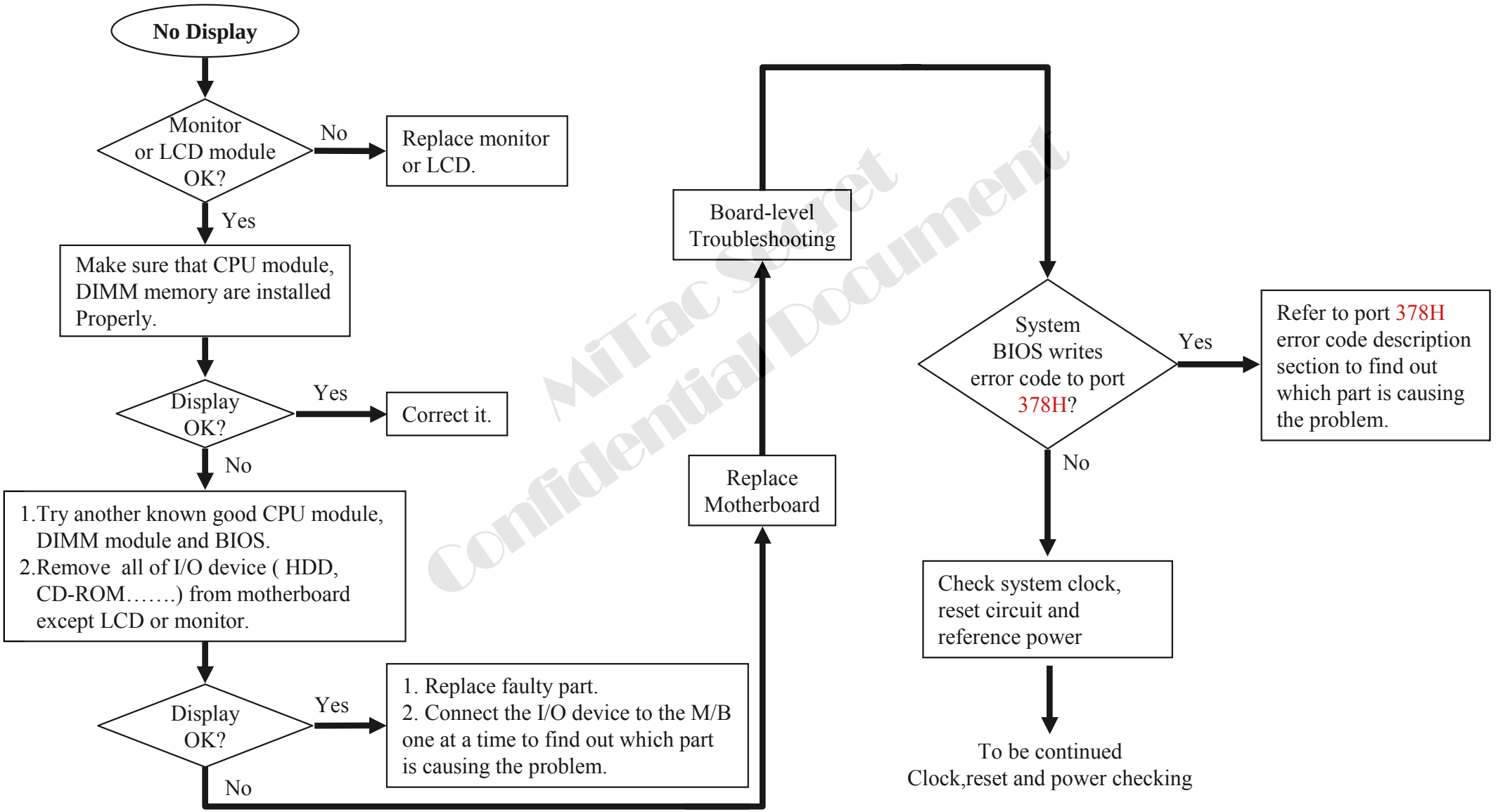
When the power button is pressed, nothing happens, no fan activity is heard and power indicator is not light up.

Power Controller



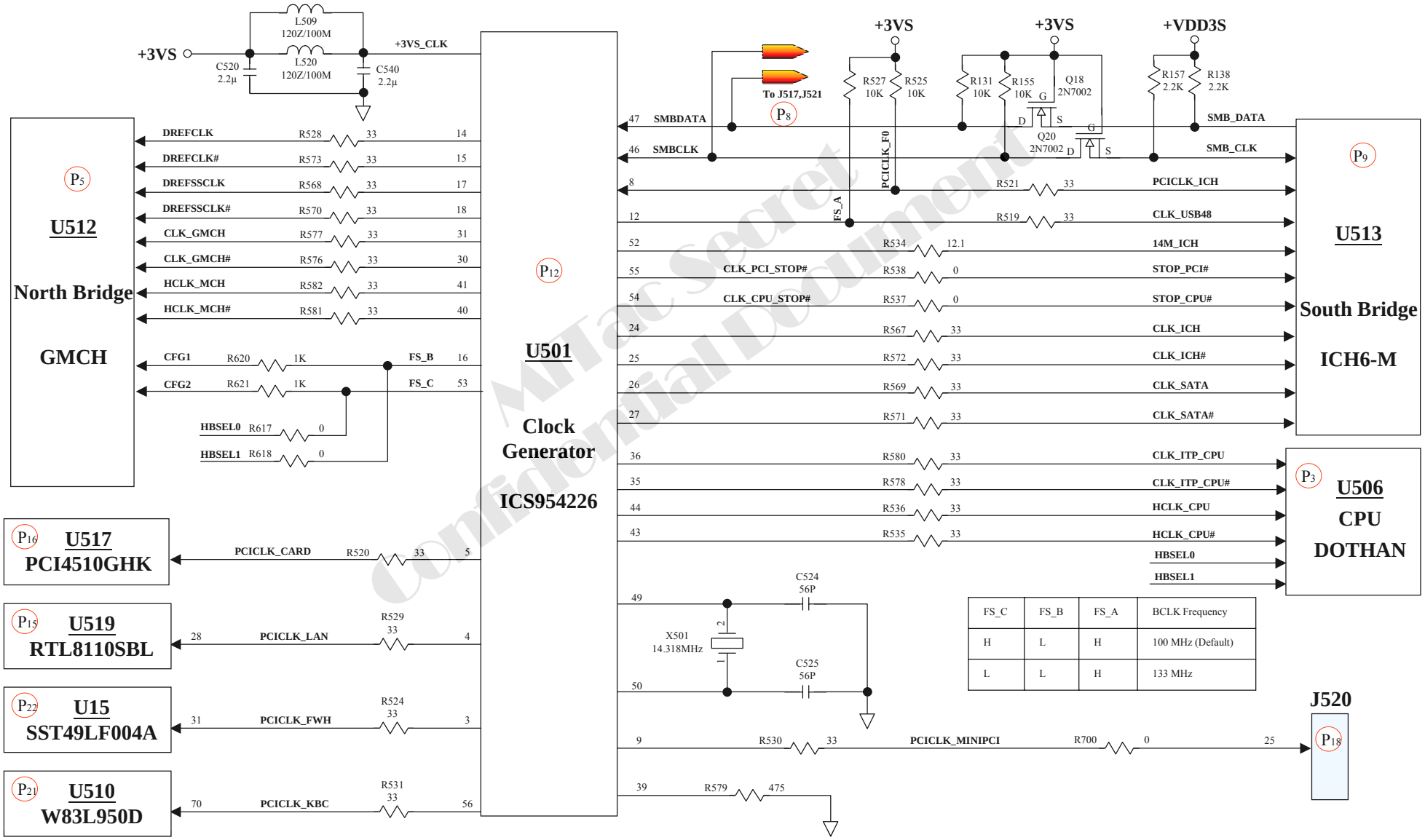
8.2 No Display-1

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.



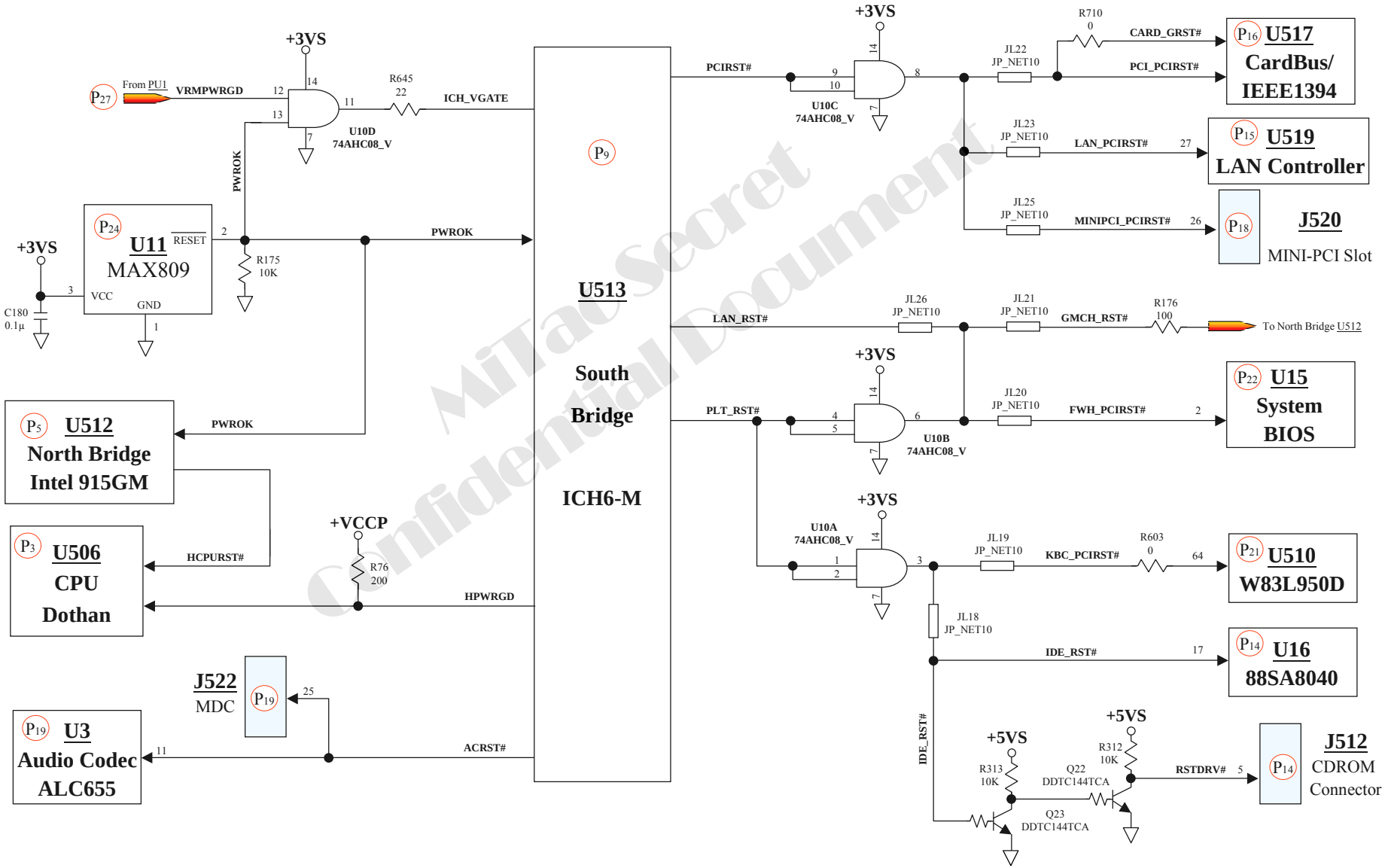
8.2 No Display-2

****** System Clock Check ******



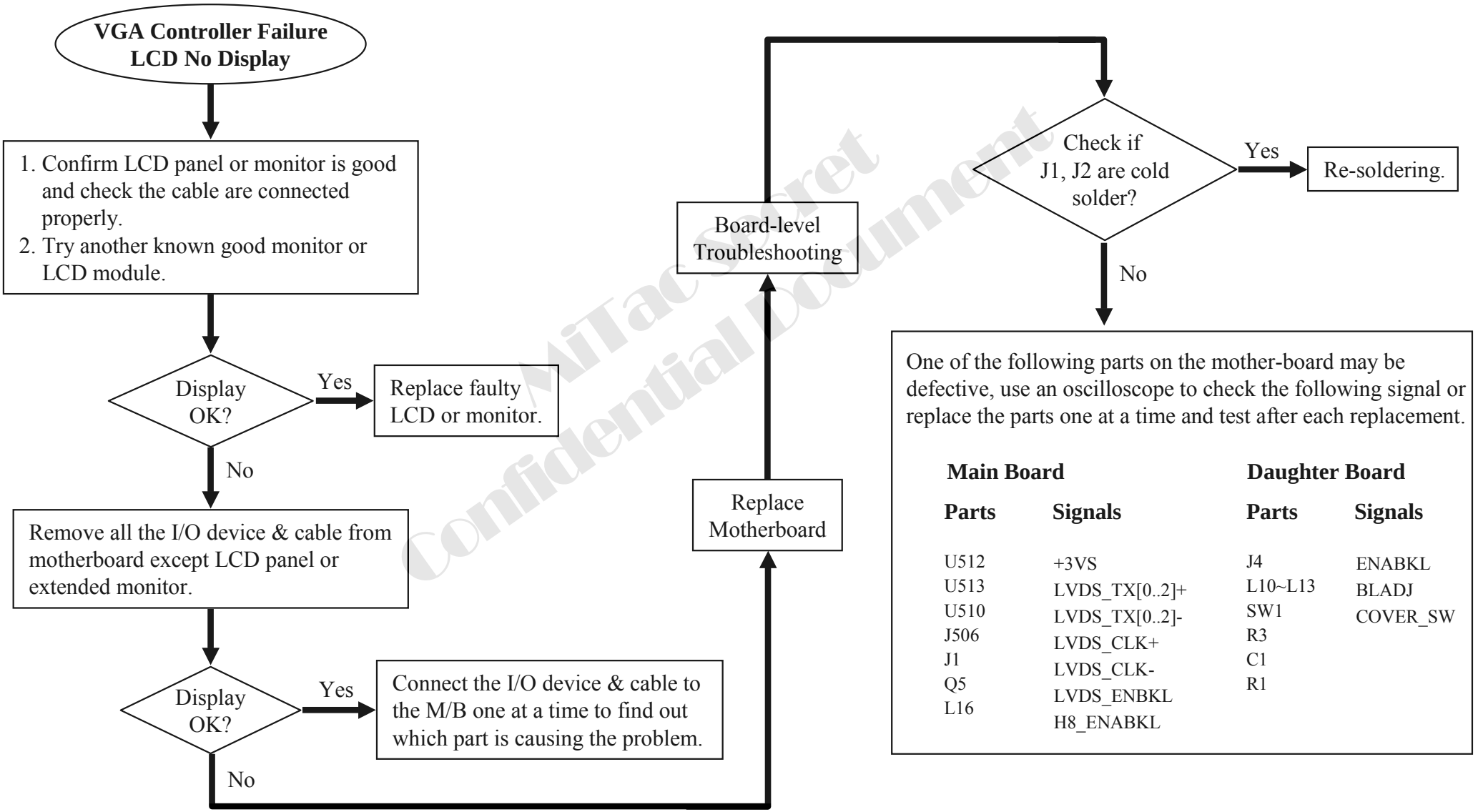
8.2 No Display-3

****** Power Good & Reset Circuit Check ******



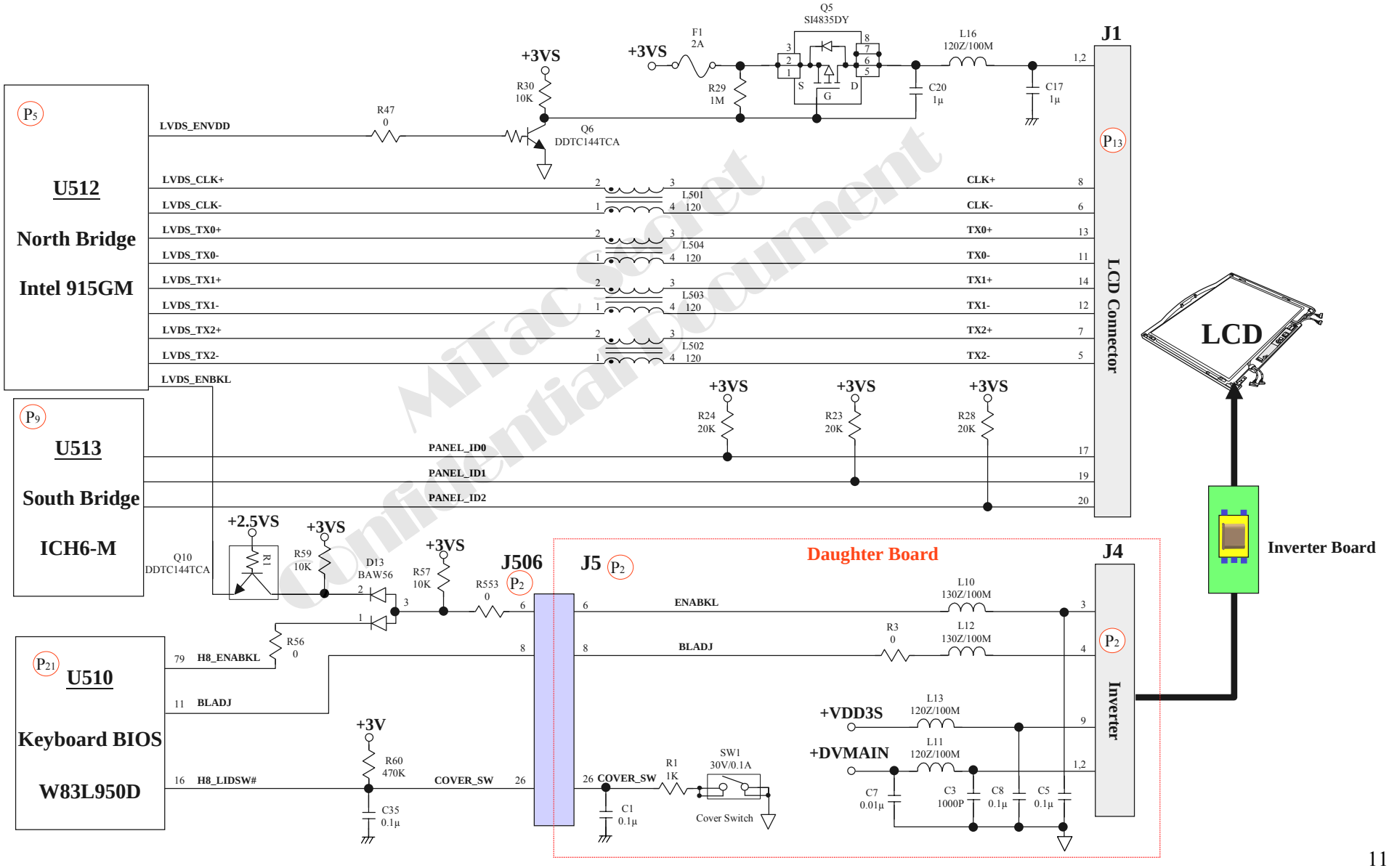
8.3 VGA Controller Failure LCD No Display-1

There is no display or picture abnormal on LCD although power-on-self-test is passed.



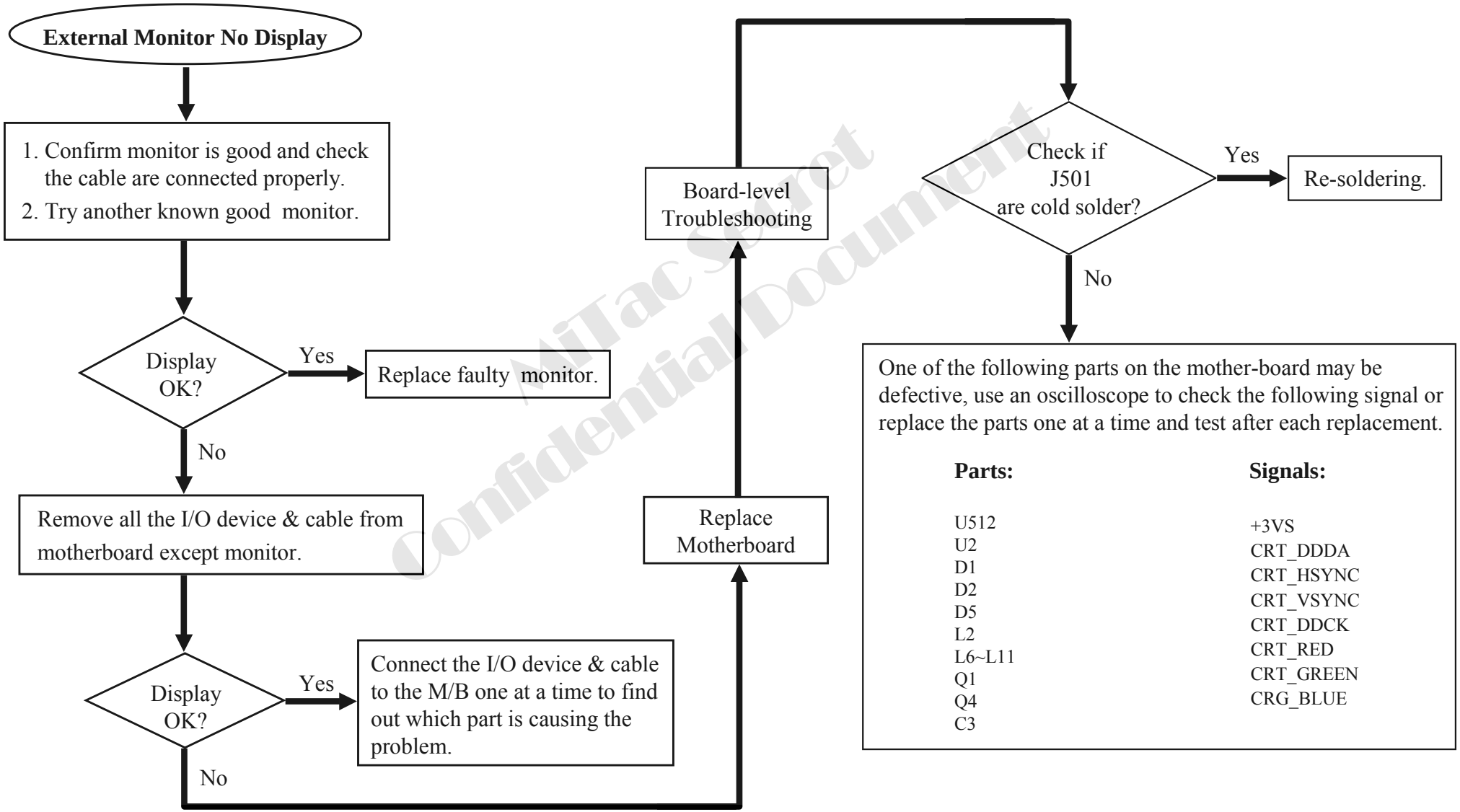
8.3 VGA Controller Failure LCD No Display-2

There is no display or picture abnormal on LCD although power-on-self-test is passed.



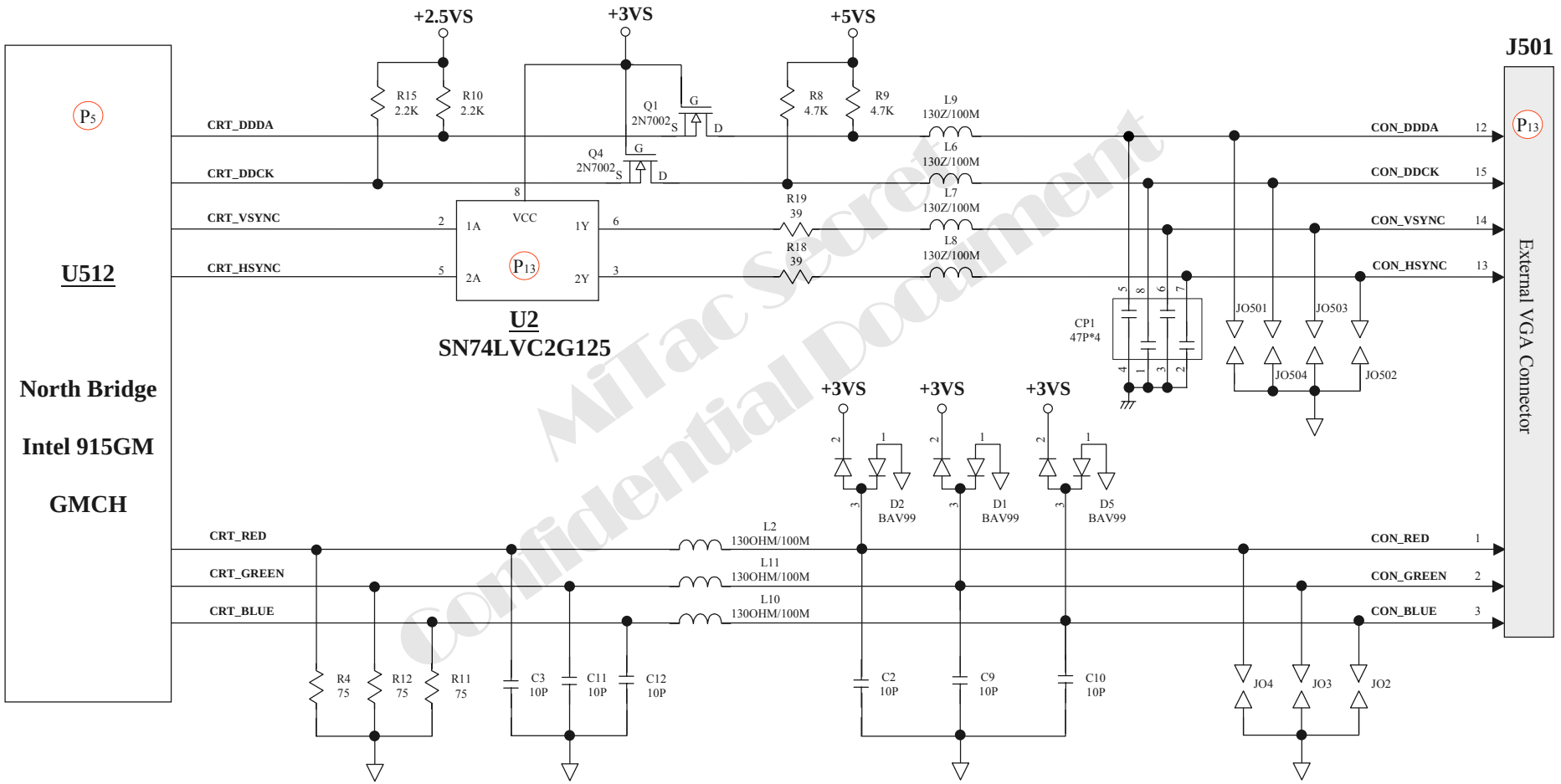
8.4 External Monitor No Display-1

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



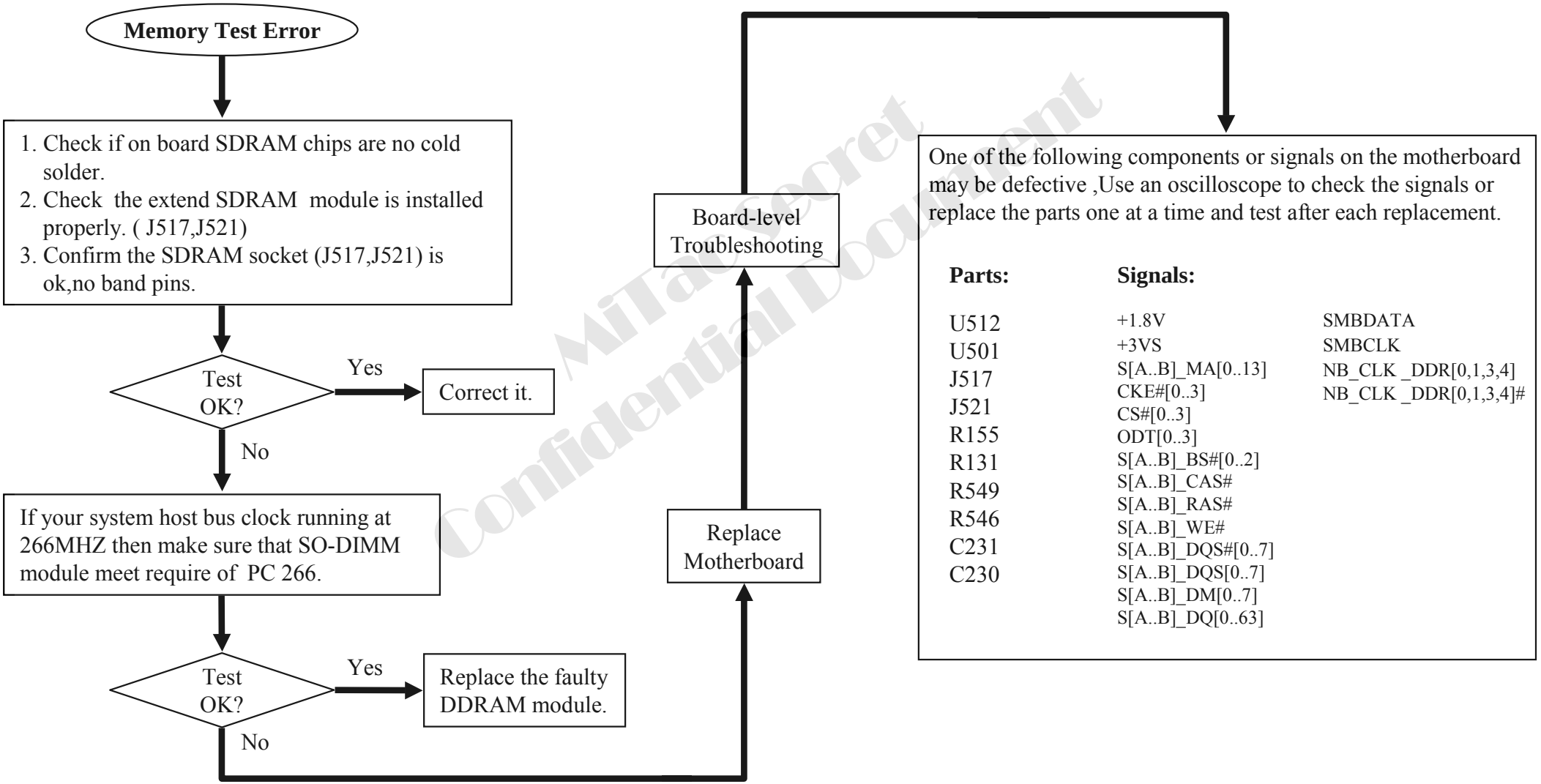
8.4 External Monitor No Display-2

There is no display or picture abnormal on CRT monitor, but it is OK for LCD.



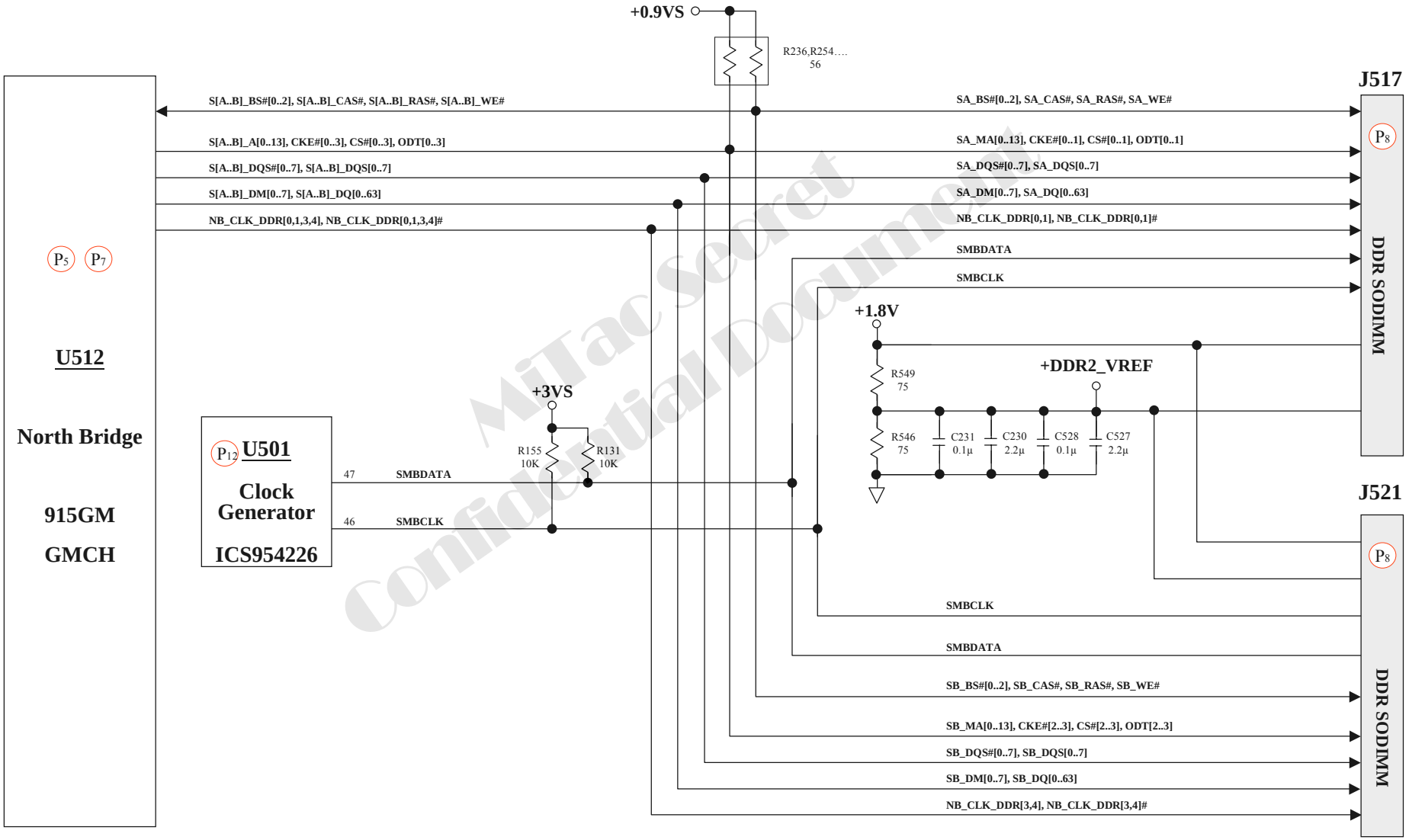
8.5 Memory Test Error-1

Extend DDRAM is failure or system hangs up.



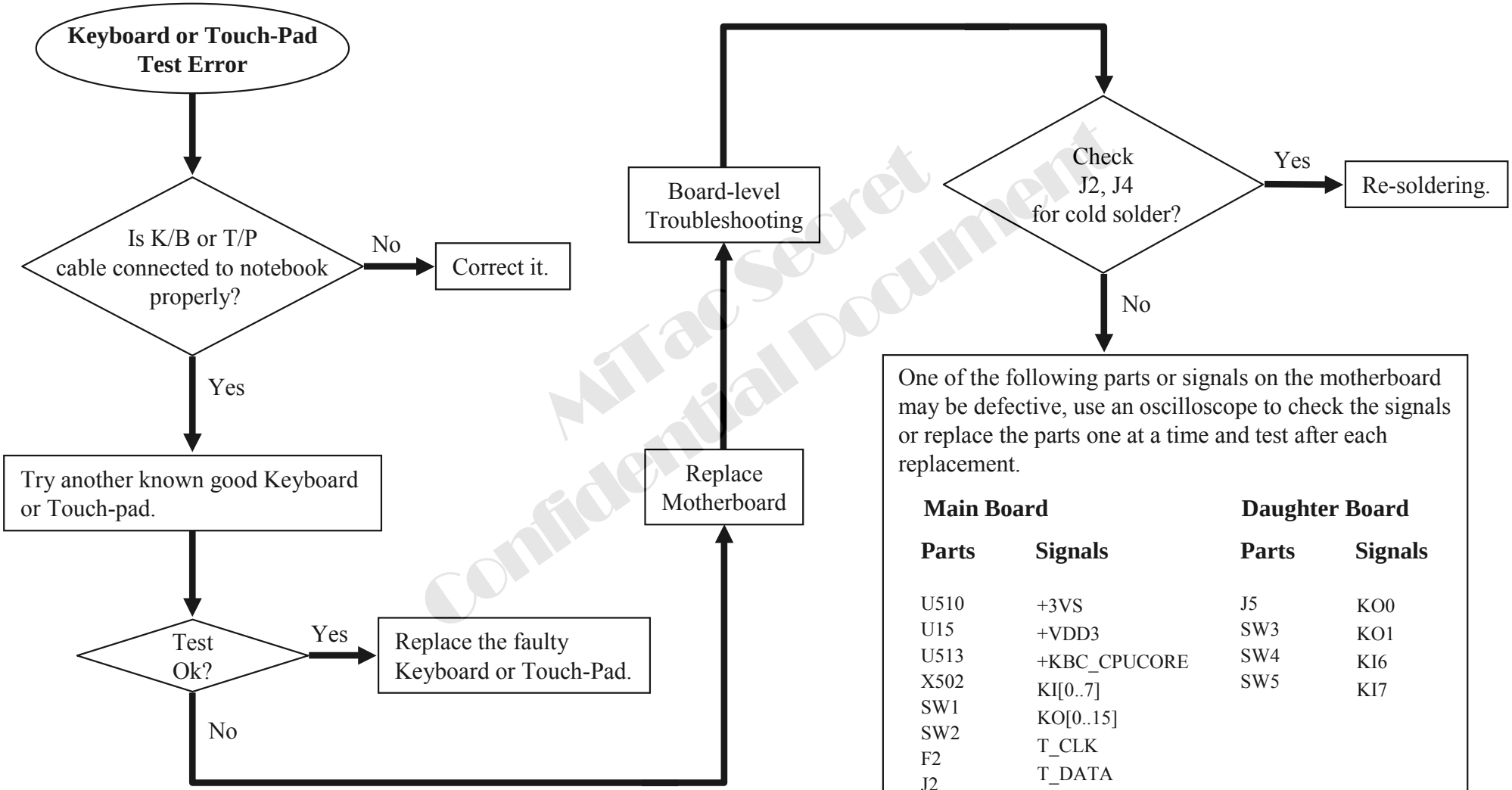
8.5 Memory Test Error-2

Extend DDRAM is failure or system hangs up.



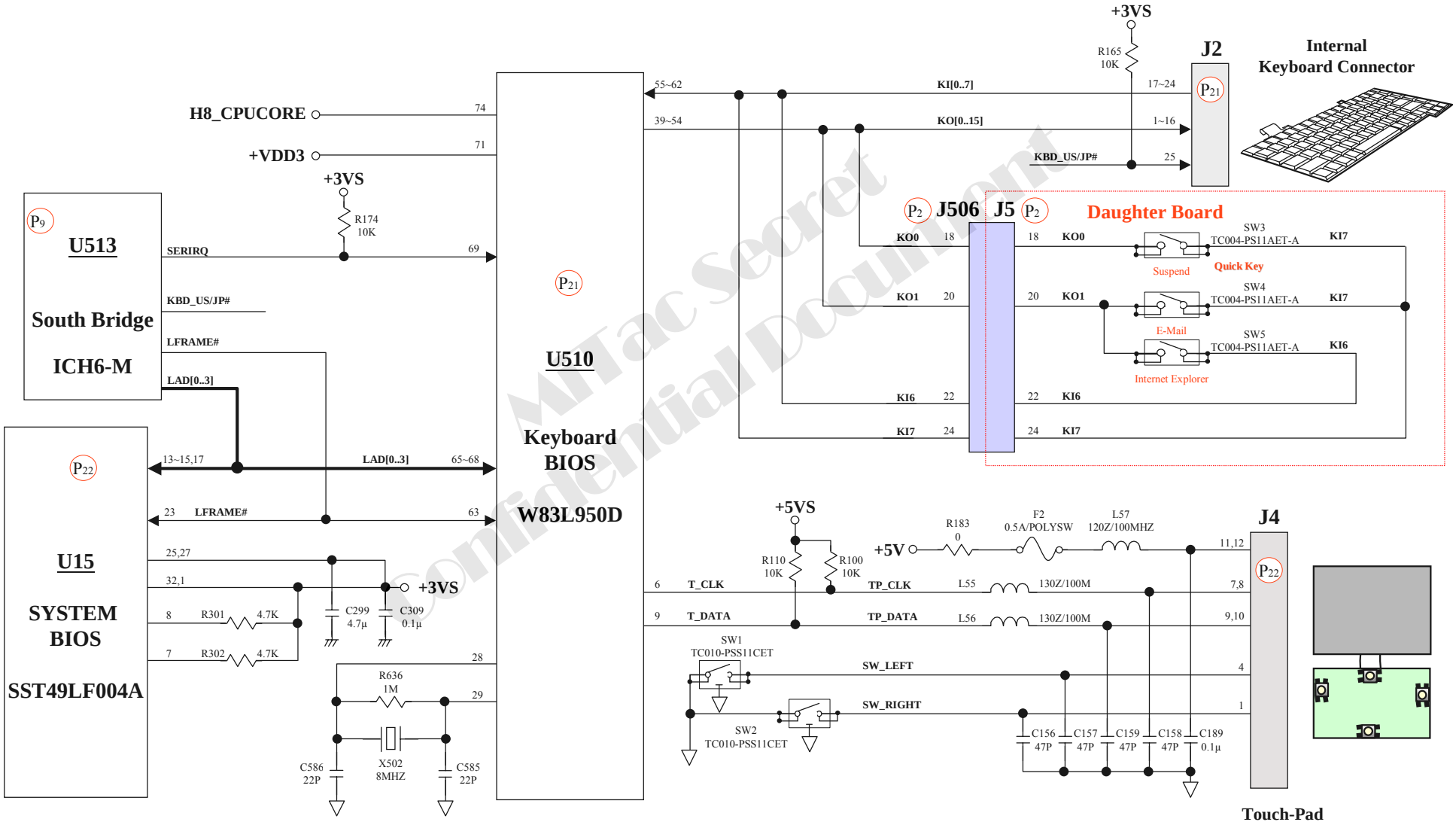
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error-1

Error message of keyboard or touch-pad failure is shown or any key does not work.



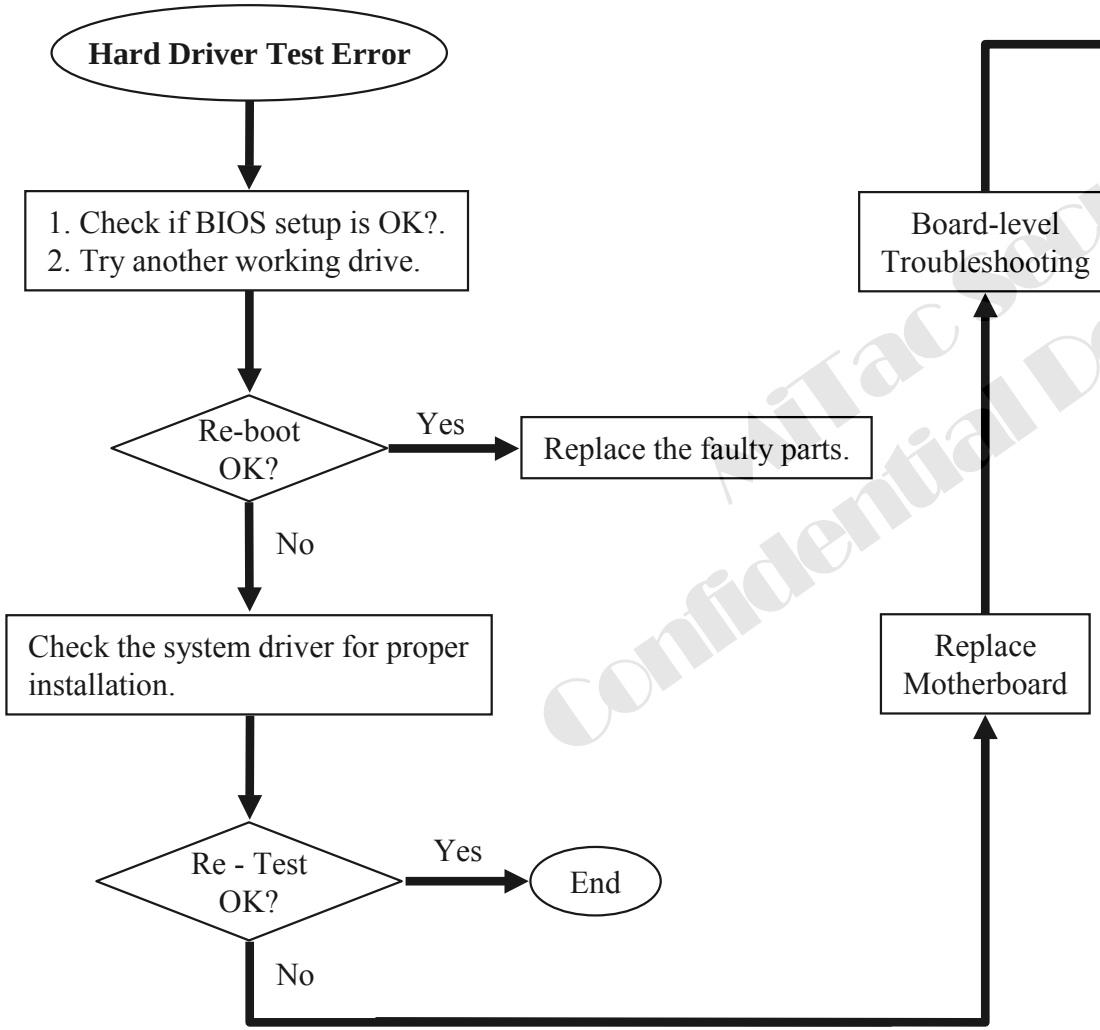
8.6 Keyboard (K/B) Touch-Pad (T/P) Test Error-2

Error message of keyboard or touch-pad failure is shown or any key does not work.



8.7 Hard Driver Test Error-1

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.

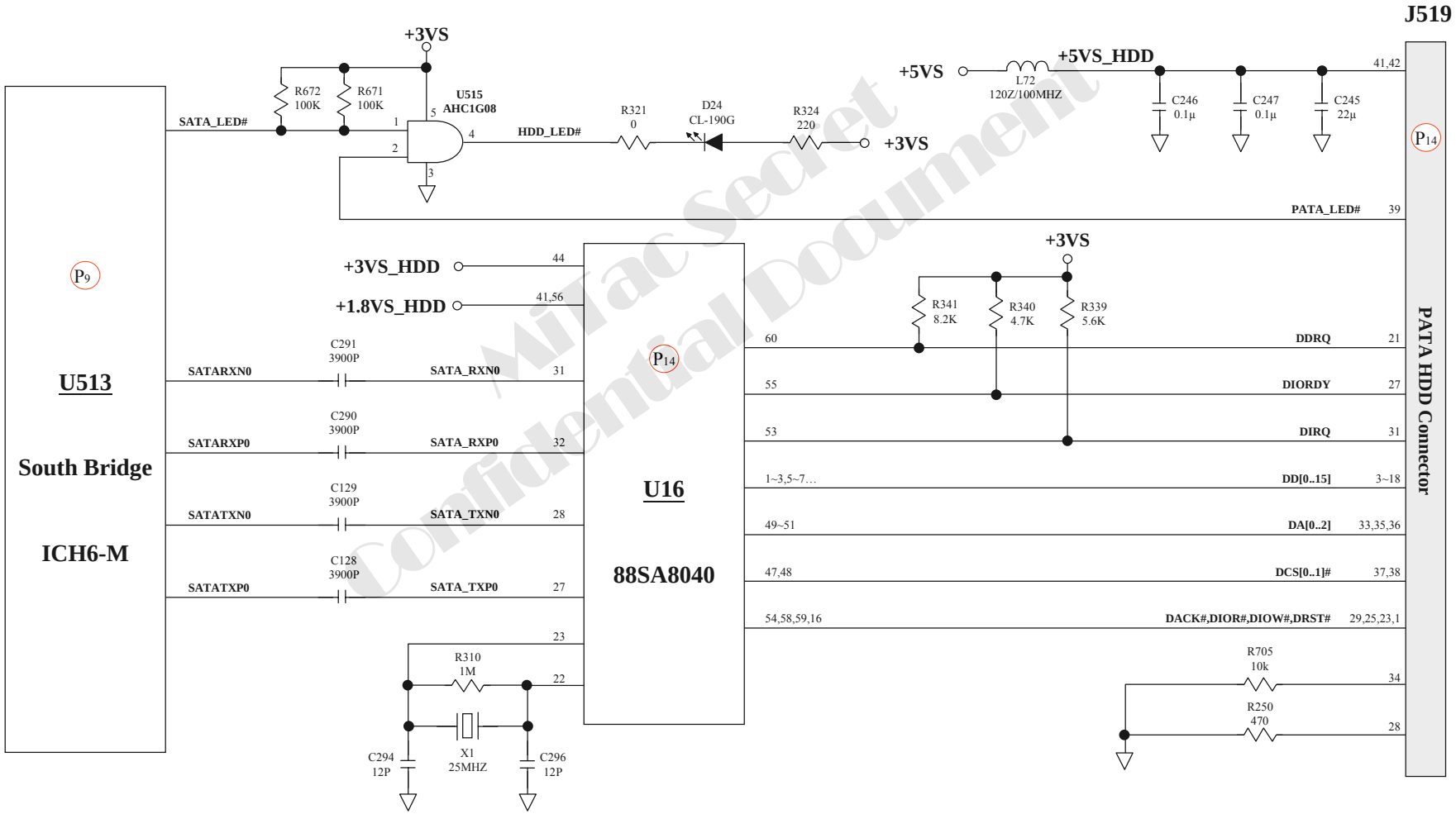


One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	Signals:
U513	+5VS
U16	+5VS_HDD
J519	SATARXN0
U515	SATARXP0
X1	SATATXN0
L72	SATATXP0
D24	DDRQ
C291	DIORDY
C290	DIRQ
C129	DD[0..15]
C128	DA[0..2]
	DCS[0..1]#

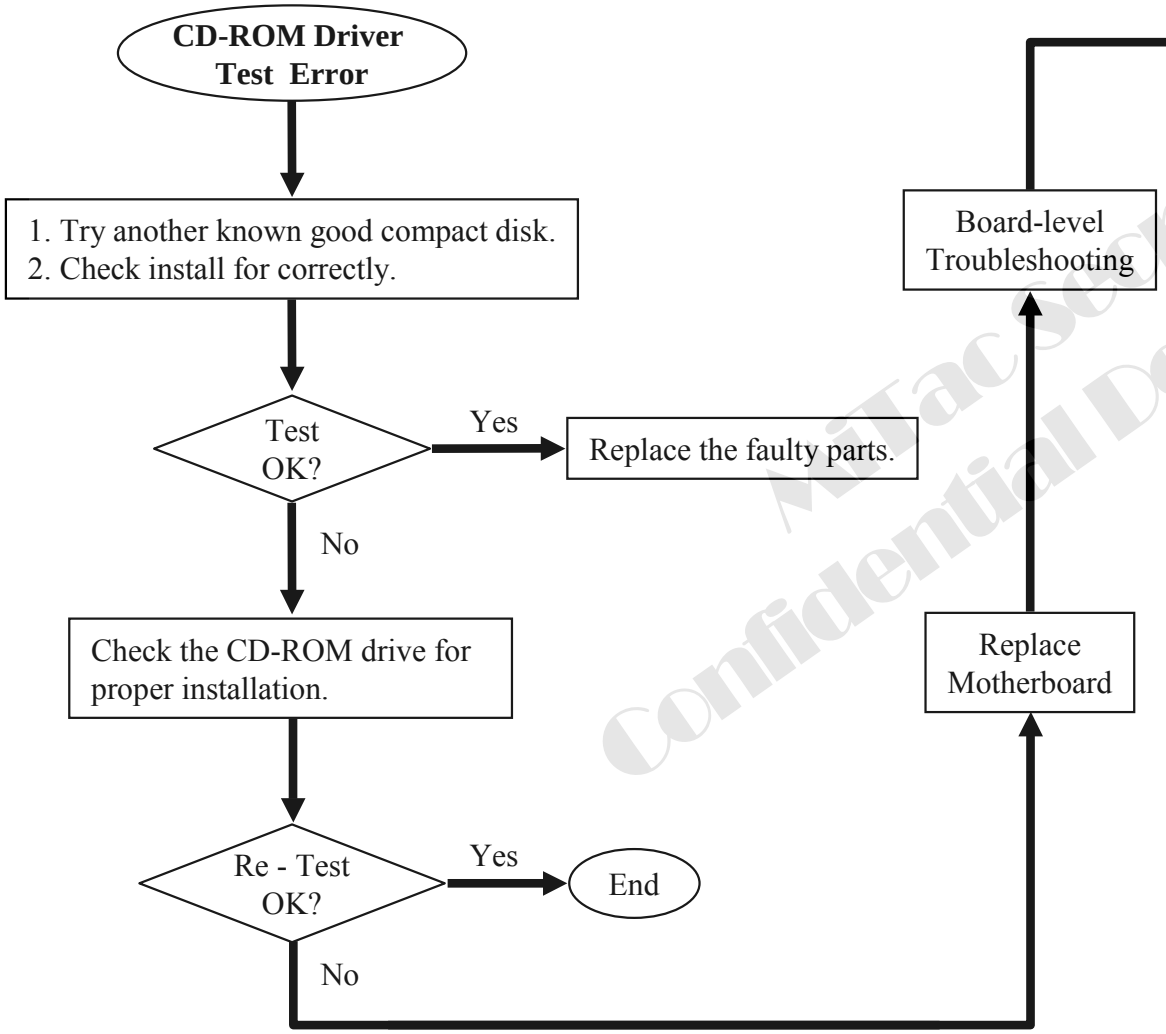
8.7 Hard Driver Test Error-2

Either an error message is shown, or the drive motor spins non-stop, while reading data from or writing data to hard disk.



8.8 CD-ROM Driver Test Error-1

An error message is shown when reading data from CD-ROM drive.

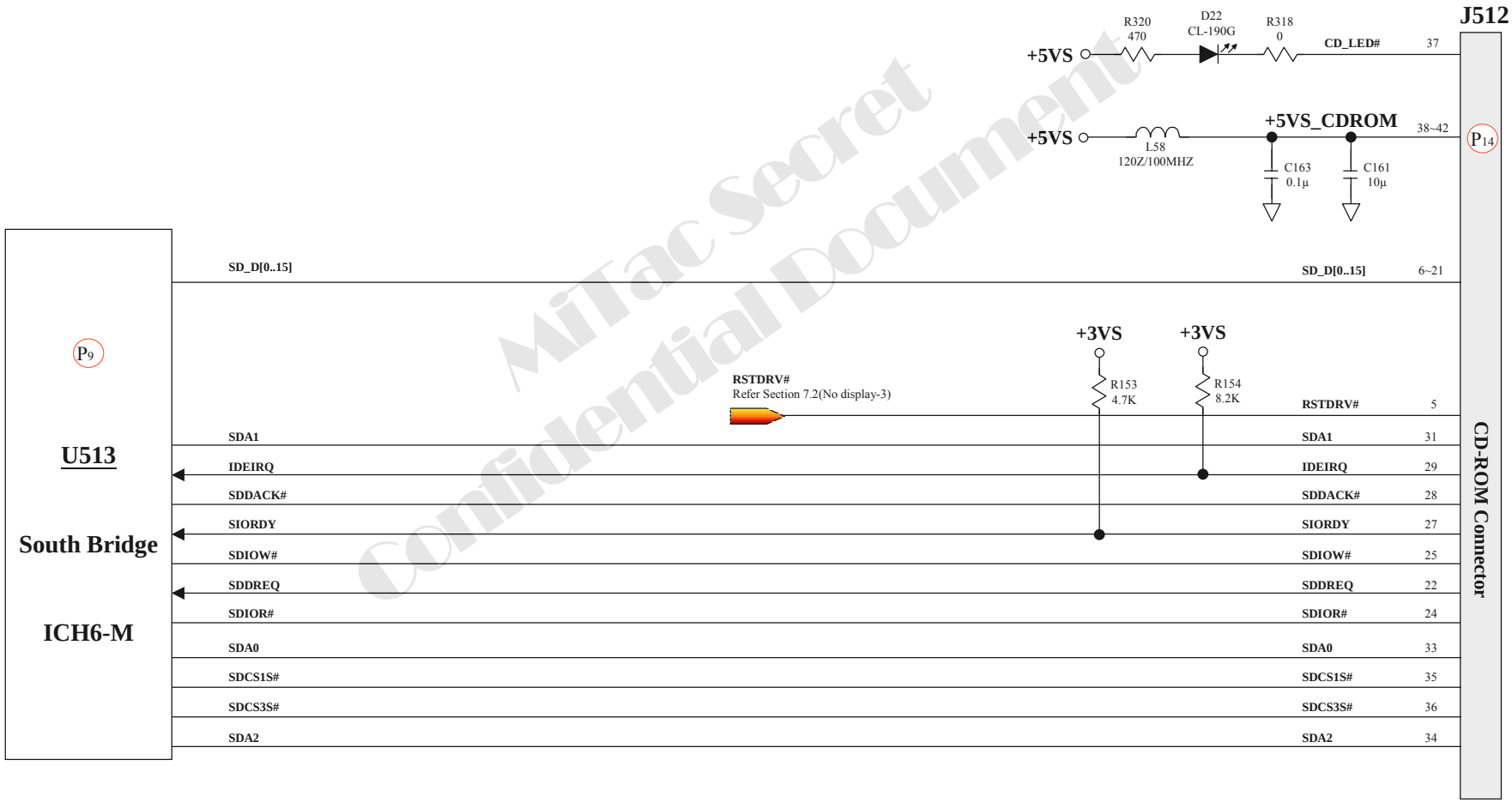


One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:	**Signals:**
U513	+5VS
J512	+5VS_CDROM
L58	SD_D[0..15]
D22	SDA1
R318	IDEIRQ
R320	SDDACK#
R154	SIORDY
R153	SDIOW#
	SDDREQ
	SDIOR#
	SDA0
	SDCS1S#
	SDCS3S#
	SDA2

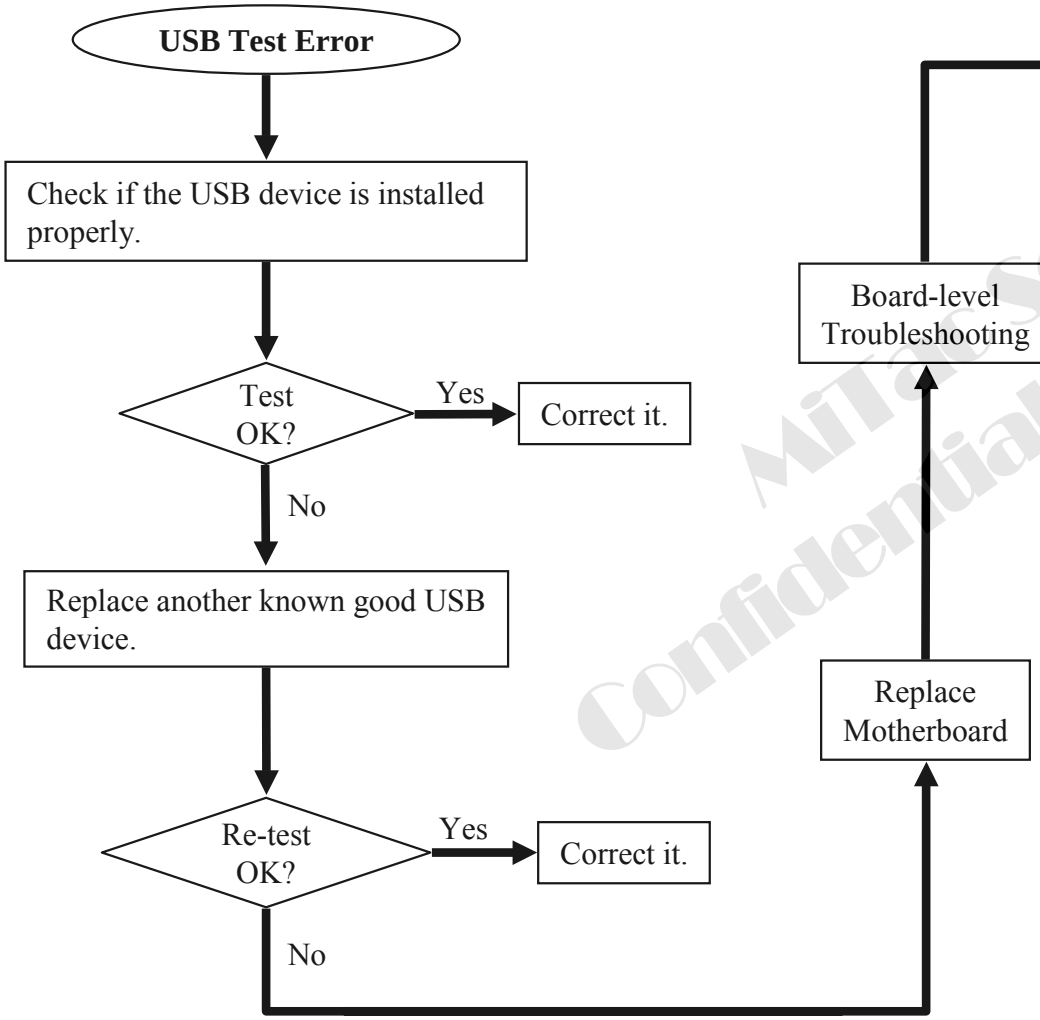
8.8 CD-ROM Driver Test Error-2

An error message is shown when reading data from CD-ROM drive.



8.9 USB Test Error-1

An error occurs when a USB I/O device is installed.

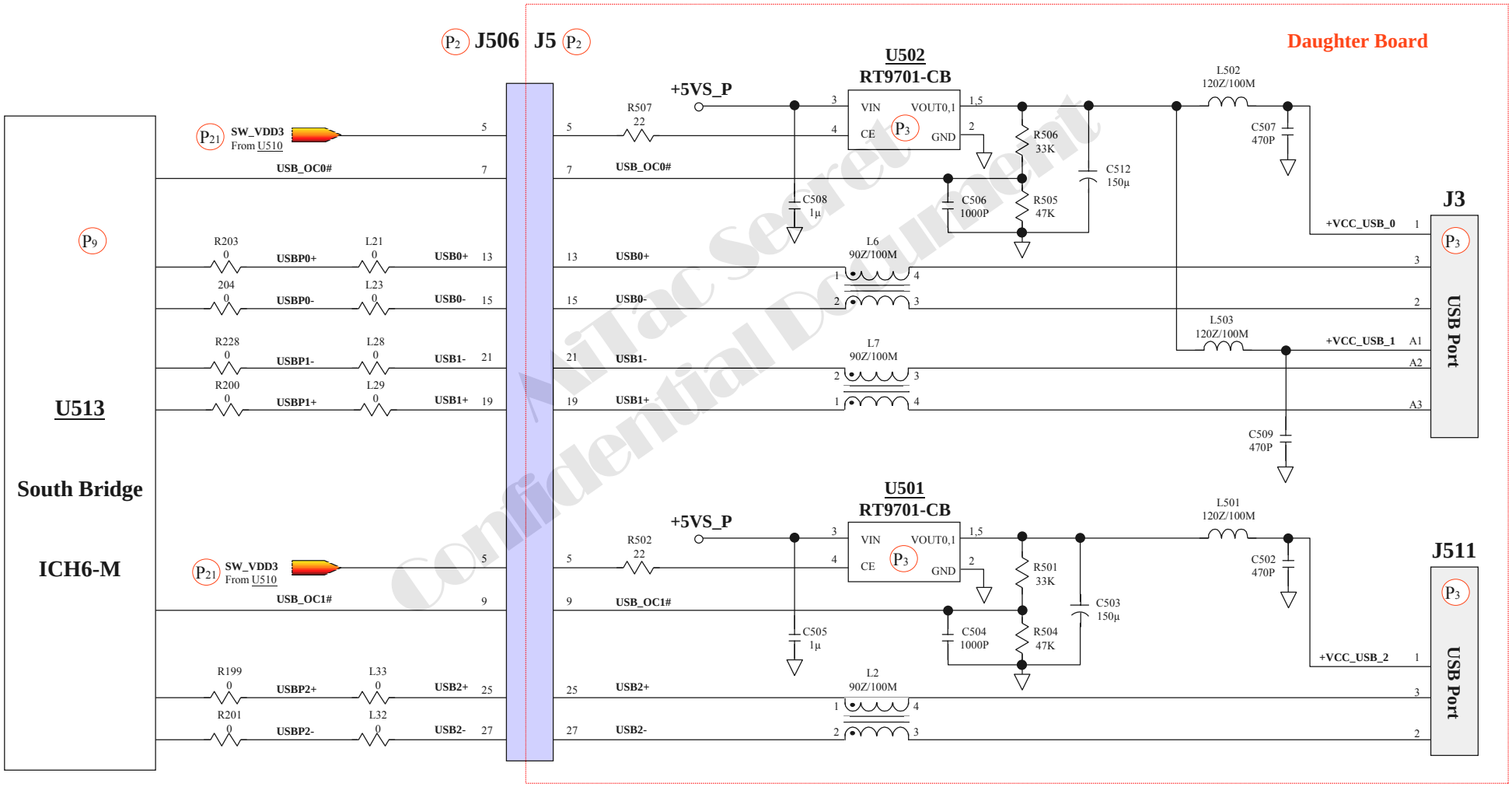


Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Main Board		Daughter Board	
Parts:	**Signals:**	**Parts:**	**Signals:**
U513	USB_OC0#	U502	+5VS_P
R203	USB_OC1#	U501	USB_OC0#
R204	USBP[0..2]+	J3	USB_OC1#
R199	USBP[0..2]-	J511	USB[0..2]+
R201	USB[0..2]+	L6	USB[0..2]-
L21	USB[0..2]-	L7	+VCC_USB_0
L23		L2	+VCC_USB_1
L28		L502	+VCC_USB_2
L29		L501	
L33		L503	

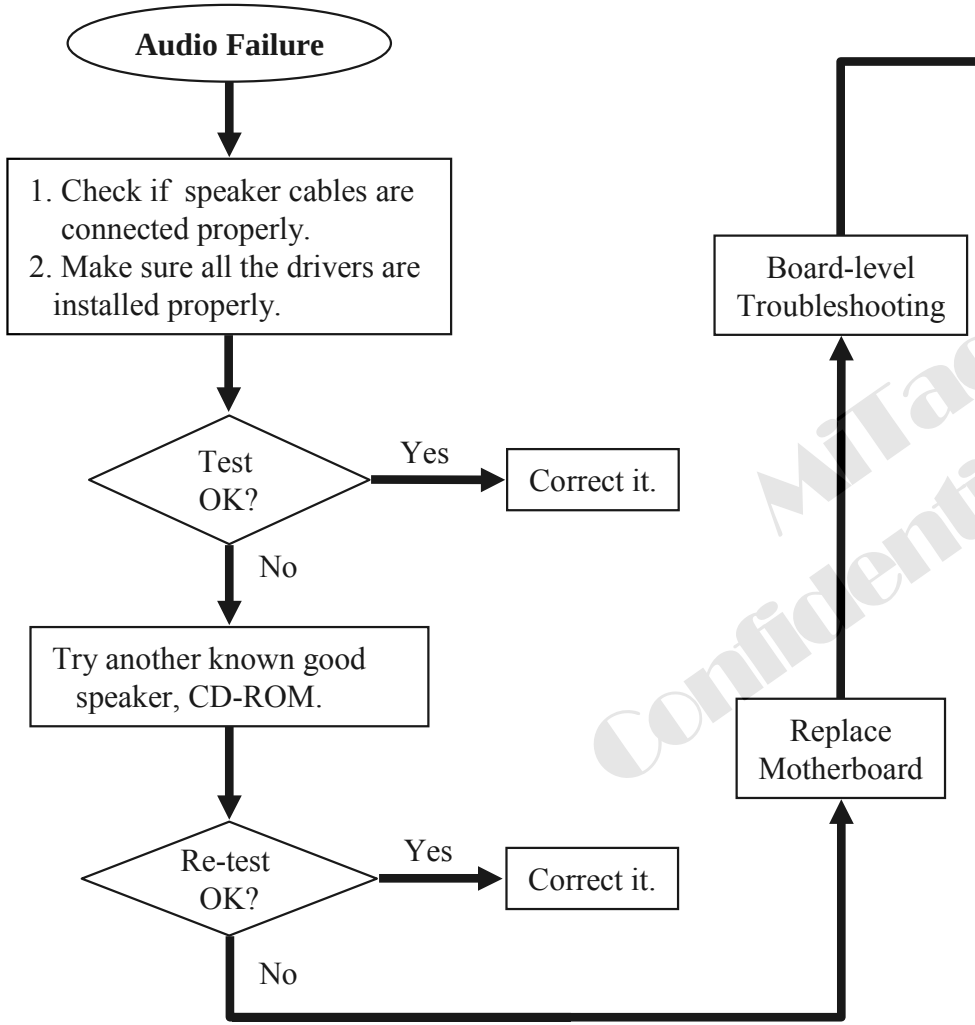
8.9 USB Test Error-2

An error occurs when a USB I/O device is installed.



8.10 Audio Failure-1

No sound from speaker after audio driver is installed.



Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1.If no sound cause of line out, check the following parts & signals:

Parts:	Signals:
U513	AMP_RIGHT
U3	AMP_LEFT
U5	DEVICE_DECT
J509	DECT_HP#OPT
J510	SPDIFOUT
J505	SPK_OFF
L12	EAPD
L13	OPTIN#
Q8	
L17	
L18	
L15	
Q7	

2. If no sound cause of MIC, check the following parts & signals:

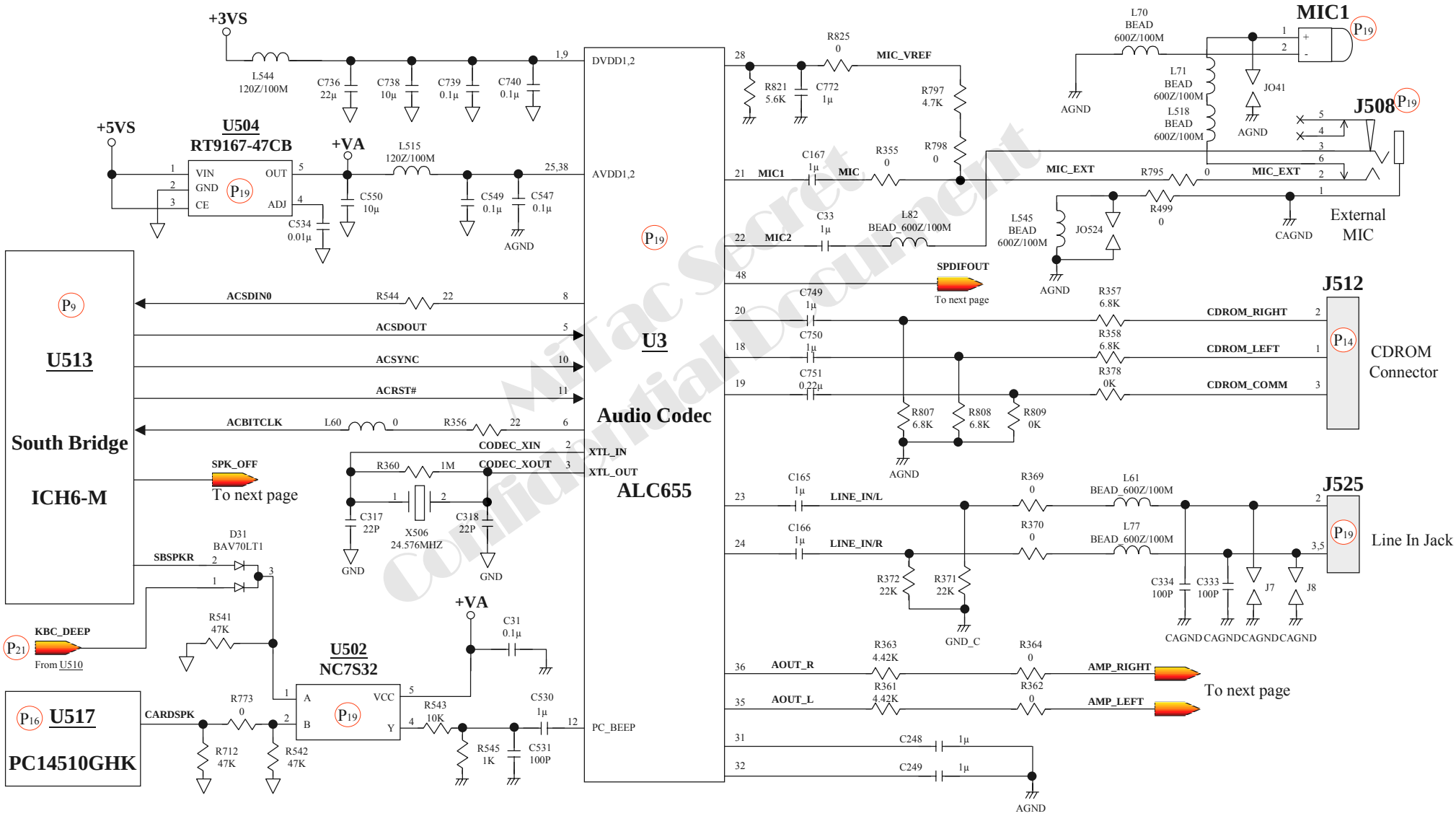
Parts:	Signals:
U513	+5VS
U3	+3VS
U504	+VA
U517	MIC_VREF
U502	MIC1
X506	MIC2
MIC1	MIC_EXT
J508	
L82	
L70	
D31	

3. If no sound cause of CD-ROM, check the following parts & signals:

Parts:	Signals:
U513	CDROM_LEFT
U517	CDROM_RIGHT
U502	CD_COMM
U3	
J512	
X506	
R357	
R358	
R378	
C749	
C750	

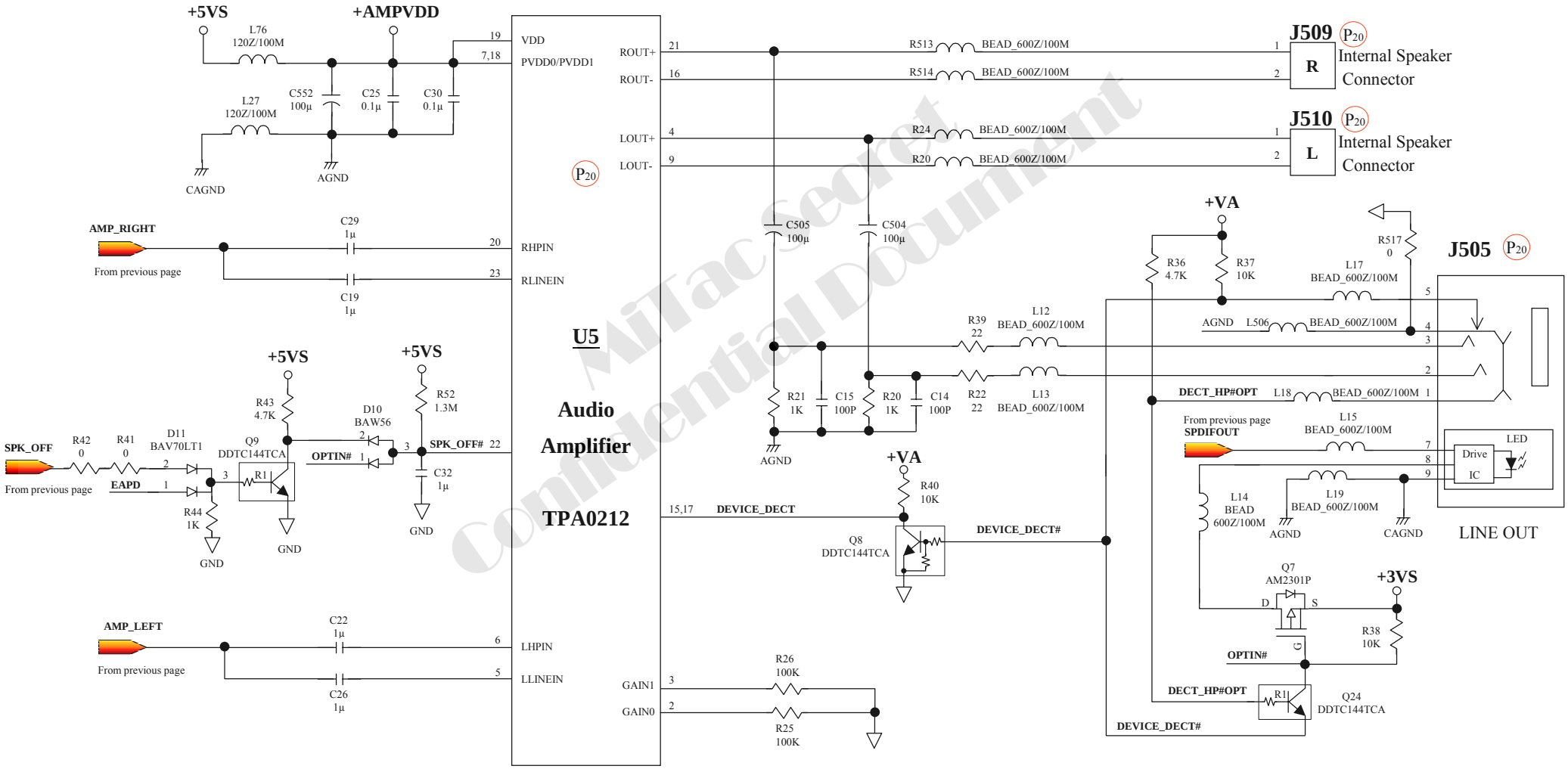
8.10 Audio Failure-2 (Audio In)

No sound from speaker after audio driver is installed.



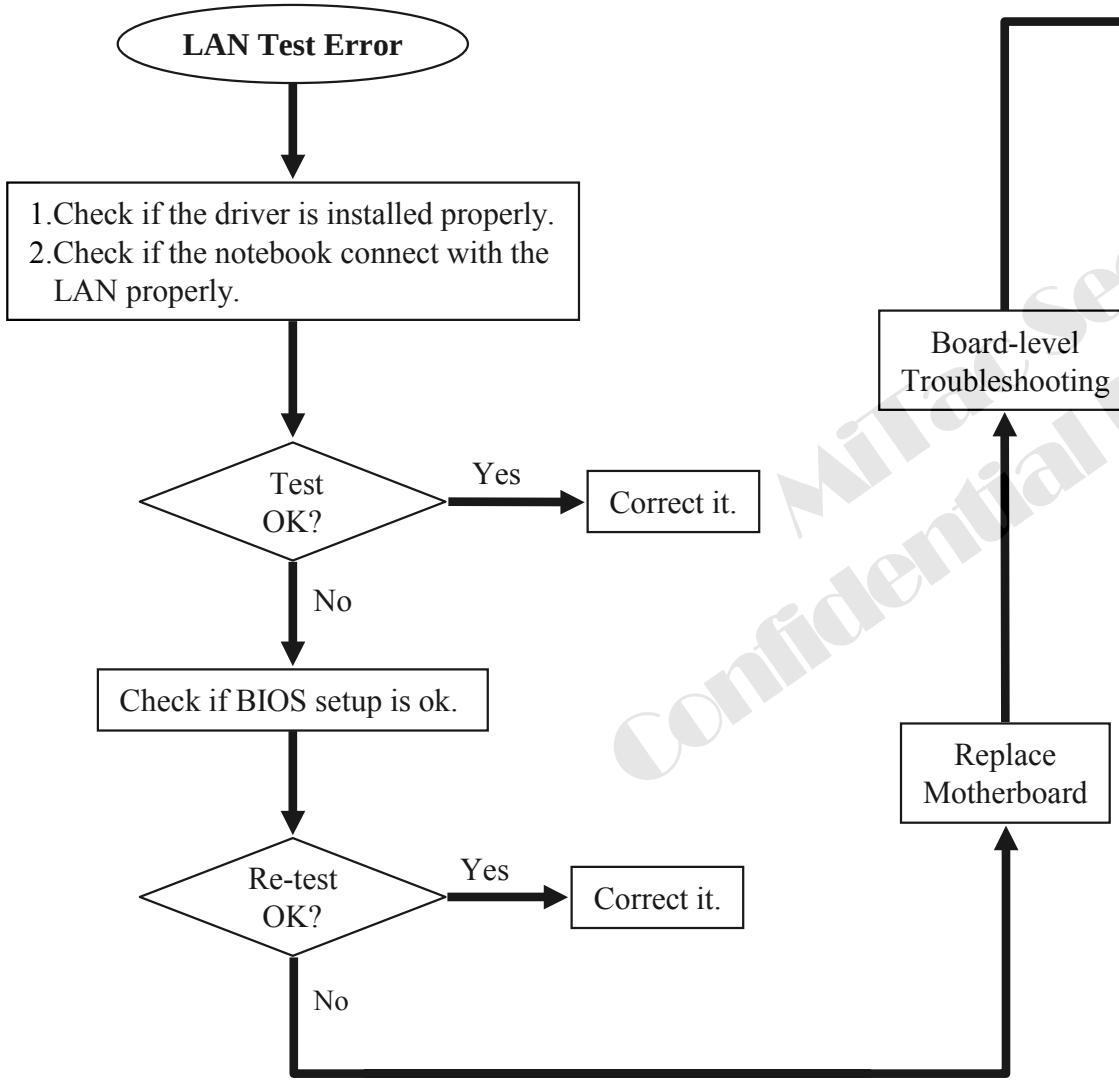
8.10 Audio Failure-3 (Audio Out)

No sound from speaker after audio driver is installed.



8.11 LAN Test Error-1

An error occurs when a LAN device is installed.

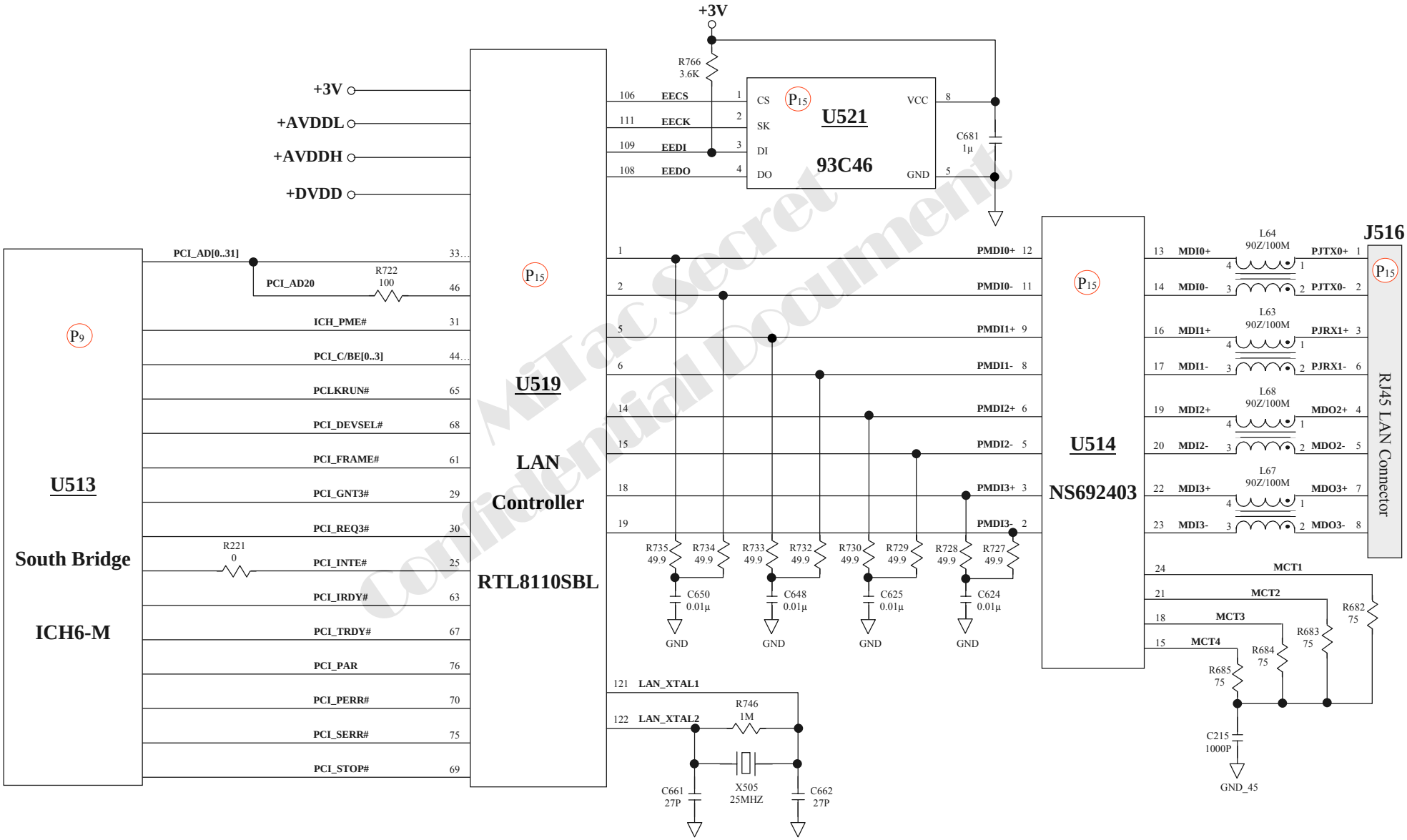


Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	Signals:
U513	+3V
U519	ICH_PME#
U514	PCI_C/BE#[0..3]
J516	PCIKRUN#
U521	PCI_DEVESEL#
X505	PMDI[0..3]+
L64	PMDI[0..3]-
L63	EECS
L68	EECK
L67	EEDI
R746	EEDO
R682	PCI_SERR#
R727	
R732	

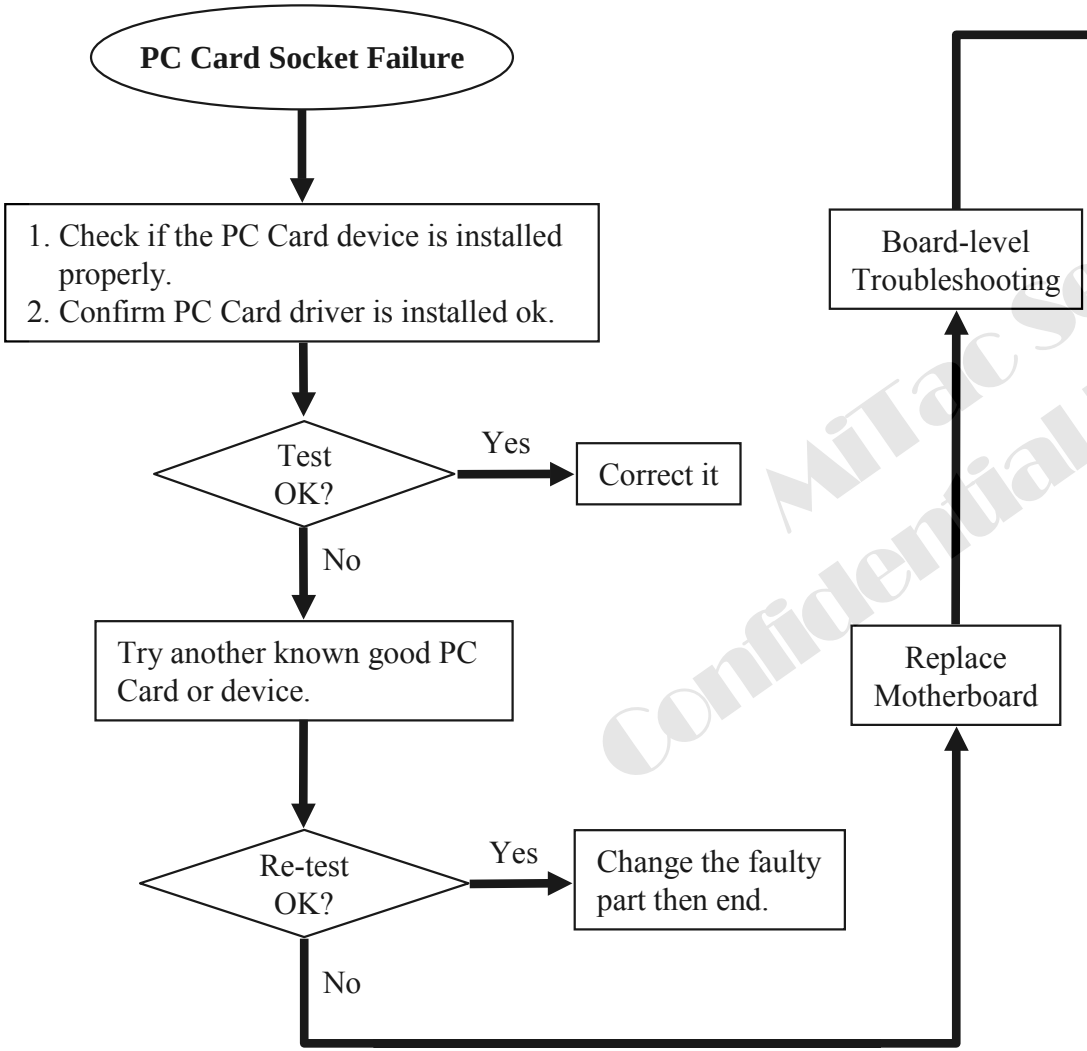
8.11 LAN Test Error-2

An error occurs when a LAN device is installed.



8.12 PC Card Socket Failure-1

An error occurs when a PC card device is installed.

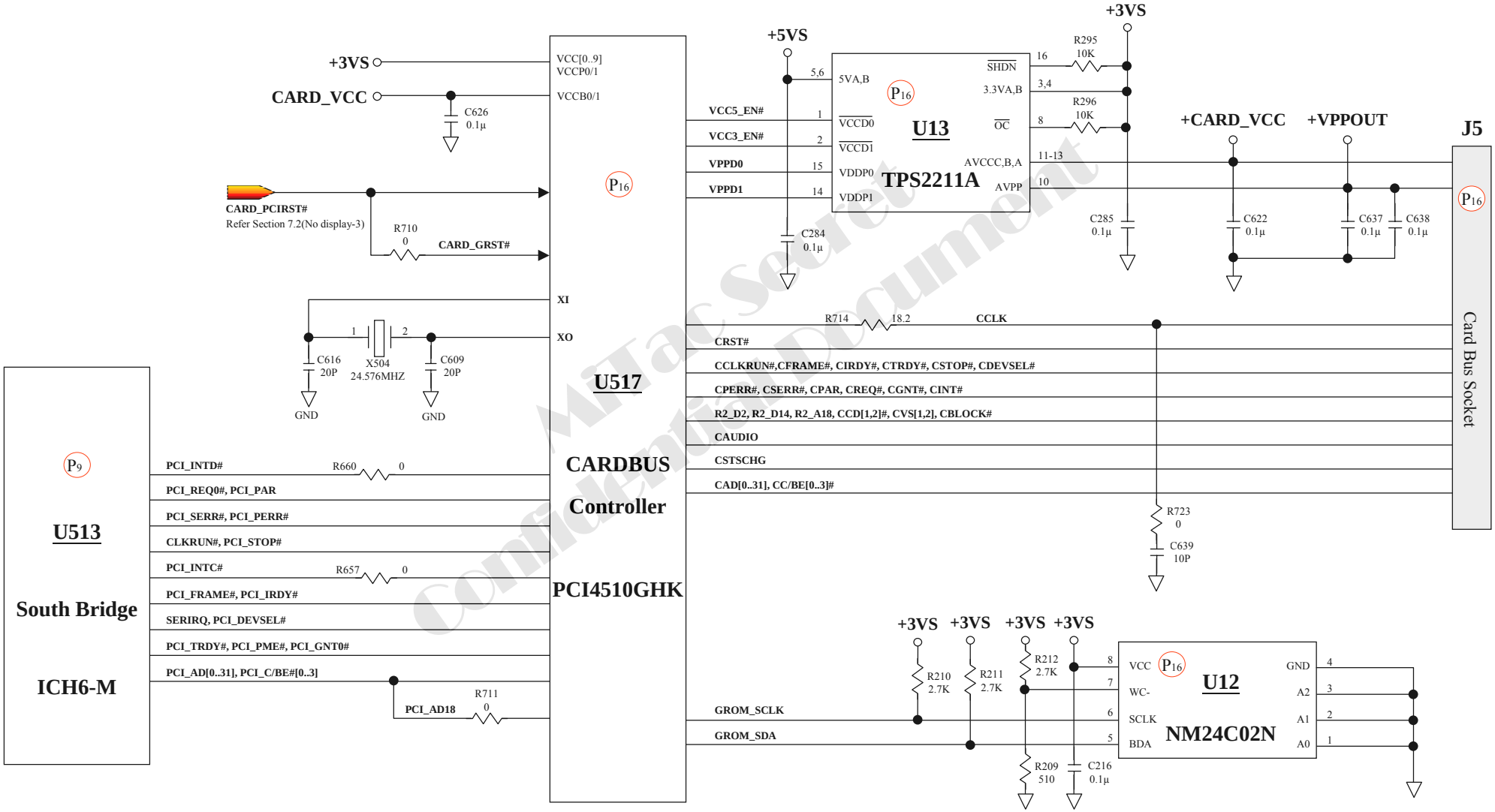


Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:	**Signals**	
U513	CARD_GRST#	PIC_PAR
U517	PCI_REQ0#	SERIRQ
U13	PCI_SERR#	PCI_AD[0..31]
J15	PCI_PERR#	PCI_C/BE#[0..3]
U12	PCI_DEVSEL#	VCC5_EN#
X504	PCI_FRAME#	VCC3_EN#
R711	PCI_IRDY#	VPPD0
R714	PCI_TRDY#	VPPD1
C639	PCI_STOP#	
C216	CLKRUN#	
R295	PCI_PME#	
R212	PCI_GNT0#	

8.12 PC Card Socket Failure-2

An error occurs when a PC card device is installed.



9. Spare Part List-1

Part Number	Description	Location(S)
526268692001	LTXXNON;8066MP/T5I3/OCP6D/1XUINB	
324180786768	IC;CPU,BANIAS DOTHAN,1.7GHZ,2MB,MICRO-FCPGA,479P,INTEL	
416268692001	LF PF;15",HT15X34-110,HYDIS,8066MP	
441686900003	LCD ASSY;15",HYDIS,HT15X34-110 TFT,8066	
413000020470	LCD;HT15X34-110 TFT,15",LVDS,XGA,HYDIS	
412682200001	PCB ASSY;INVERTER BD,DA-1A08-B,PWR	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
624200010140	LABEL;5*20,BLANK,COMMON	
411682200001	PWA;PWA-INVERTER BD,DA-1A08-B,PWR	
411682200002	PWA;PWA-INVERTER BD,SMT,DA-1A08-B,PWR	
411682200003	PWA;PWA-INVERTER BD,SMT TOP,DA-1A08-B,PWR	
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R17
271071202301	RES;2K ,1/16W,5% ,0603,SMT	R12
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R13,R3
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R16,R20,R22
271071432111	RES;4.32K,1/16W,1% ,0603,SMT	R10
271071563101	RES;56K ,1/16W,1% ,0603,SMT	R6
271072474101	RES;470K ,1/10W,1% ,0603,SMT	R4
272012105401	CAP;1U ,CR,16V ,10%,1206,X7R,SMT	C14A,C14B
272023475401	CAP;4.7U ,25V ,10%,1210,X5R,SMT	C1
272030050302	CAP;5P,3KV,5%,1808,NPO,SMT,only HolyStone	C19
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SMT	C16,C17,C6
272073223401	CAP;.022U,CR,25V ,10%,0603,X7R,SMT	C9
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,SMT	C11
272075222401	CAP;2200P,50V ,10%,0603,X7R,SMT	C15A

Part Number	Description	Location(S)
291000000203	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM02B,only A	J2
291000020204	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SMO2B	
294011200043	LED;RE/GR,H0.8,L1.9,W1.6,19-22SRVGC	LED1
291000021104	CON;HDR,MA,11P*1,1.25,R/A,3811Y-T011-NNNA,S	CN1
291000020221	CON;HDR,MA,11P*1,1.25MM,R/A,ACES,85204-1100,SMT,PWR	
294011200069	LED;GREEN,19-21VGC/TR8,LED_CL190,SMT,PRC	LED3,LED5
288114148004	DIODE;1N4148WS,75V,200mW,SOD-323,SMT	D1
272010680301	CAP;68P,2KV,5%,1206,NPO,SMT,only HolyStone	C18
272010680401	CAP;68P ,CR,2KV,10%,1206,NPO,SMT,PRC	
273001050126	XFMR;CI8.5,25T/2150T,292mH,Varnish Twice,SMT,c	T1
271071753301	RES;75K ,1/16W,5% ,0603,SMT	R8
411682200004	PWA;PWA-INVERTER BD,SMT BOT,DA-1A08-B,PWR	
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R11
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R7
271071152302	RES;1.5K ,1/16W,5% ,0603,SMT	R19
271071331301	RES;330 ,1/16W,5% ,0603,SMT	R18,R21,R23
271071432211	RES;43.2K,1/16W,1% ,0603,SMT	R1
271071822102	RES;8.2K ,1/16W,1% ,0603,SMT	R14B
271072474101	RES;470K ,1/10W,1% ,0603,SMT	R5
272071105403	CAP;1U ,10V ,10%,0603,X5R,SMT	C10,C4
272071332401	CAP;.33U ,10V ,10%,0603,X7R,SMT	C2
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SMT	C12
272075101401	CAP;100P ,50V ,10%,0603,COG,SMT	C20,C21
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,SMT	C13,C3,C8
281101015001	IC;MP1015EM-Z,CCFL CTRL,TSSOP20,MPS	U1

9. Spare Part List-2

Part Number	Description	Location(S)
294011200043	LED;RE/GR,H0.8,L1.9,W1.6,19-22SRVGC	LED2
295000010120	FUSE;FAST,1.5A,63V,1206,SMT,PRC	F1
295000010149	FUSE;FAST,1.5A,63VDC,1206,SMT,043301.5	
316682200001	PCB;PWA-INVERTER BD (DA-1A08-B);PWR	R0E
361200003047	SOLDER PASTE;NO CLEAN,RMA,CK3000-2	
294011200069	LED;GREEN,19-21VGC/TR8,LED_CL190,SMT,PRC	LED4,LED6
272073472301	CAP;4700P,CR,50V ,5% ,0603,X7R,SMT	C5
271071137011	RES;137 ,1/16W,1% ,0603,SMT	R14A
272073104401	CAP;.1U ,CR,25V,10%,0603,X7R,PRC	C22,C7
344600000608	BOX;PVC,T=0.5MM,PRC	
221674320005	CARTON; INVERTER, E-NOTE INVERTER BD	
451686900031	LCD ME KIT;15",8066	
342686900005	HINGE;HOUSING,LCD,L,8066	
342686900012	HINGE;L,SZS,8066	
342686900004	HINGE;HOUSING,LCD,R,8066	
342686900013	HINGE;R,SZS,8066	
342686900003	BRACKET;LCD,HOUSING,R,8066	
342686900002	BRACKET;LCD,HOUSING,L,8066	
422686900003	WLEN ASSY;CABLE,8066	
422686900002	WIRE ASSY;LCD,HSD150PX14,8066	
422686900005	WIRE ASSY;LCD,HSD150PX14,MPT,8066	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	

Part Number	Description	Location(S)
422686900004	WIRE ASSY;INVERTER,8066	
422686900006	WIRE ASSY;INVERTER,MPT,8066	
346669900004	INSULATOR;INVERTER,7170	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
346686900013	CONDUCTIVE TAPE;HOUSING,LCD,I-CABLE,8066	
345677000018	CONDUCTIVE TAPE;LCD,LYNX	
340686910002	HOUSING ASSY;LCD,ID2,8066	
340686910004	COVER ASSY;LCD,ID2,8066	
346677000012	MYLAR;COVER,LCD,LYNX	
431686920001	CASE KIT;PATA,8066MP	
451686920051	HOUSING KIT;8066	
340686900011	SPEAKER ASSY;L,8066	
340686900012	SPEAKER ASSY;VECO,L,8066	
340686900010	SPEAKER ASSY;R,8066	
340686900013	SPEAKER ASSY;VECO,R,8066	
340686900018	COVER ASSY;8066MP	
340686900020	HOUSING ASSY;8066MP	
340686900002	COVER ASSY;CPU,8066	
340686900003	COVER ASSY;HDD,8066	
344686900006	COVER;HINGE,8066	
340686900021	COVER ASSY;KB,8066MP	
340686900019	SHIELDING ASSY;COVER,8066MP	
370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/NLK	
371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	
371102610603	SCREW;M2.6L6,FLNG/PAN(+),NIW/NLK	

9. Spare Part List-3

Part Number	Description	Location(S)
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
422686900007	WIRE ASSY;MODEM,8066MP	
341680900001	SPC SCREW;#4-1/4,8050	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
422687600005	CABLE FFC;TP,8965	
346670500014	INSULATOR;MDC,TETRA	
344684000040	DUMMY CARD;PCMCIA,8050M	
345686300002	SPONGE;HDD,8050FX	
412678800001	PCB ASSY;FAX MODEM 56K,1456VQL4A,8381B	
451686900091	HEATSINK ME KIT;8066	
341677000002	SPRING;SCREW,HEATSINK,LYNX	
340686900006	HEATSINK ASSY;CPU,8066	
340686900017	HEATSINK ASSY;FORCECON,8066	
411686920001	PWA;PWA-8066MP,PATA,MOTHER BD	
411686920002	PWA;PWA-8066MP,PATA,MOTHER BD,T/U	
411686920003	PWA;PWA-8066MP,PATA,MOTHER BD,SMT	
271002000301	RES;0 ,1/10W,5% ,0805,SMT	L83,R183,R27,R45,R502,R53,R55
271003228101	RES;2.2 ,1/4W,1% ,0805,SMT	PR74,PR76
271012000301	RES;0 ,1/8W,5% ,1206,SMT	PR73
271045029101	RES;.02 ,1W ,1% ,2512,SMT ,only Cyntec	PR25
271586026101	RES;.02 ,2W,1%,2512,SMT	
271046017301	RES;.001,2W,5%,2512,CYNTEC,SMT	PR506
271061000002	RES;0 ,1/16W,0402,SMT	R101,R102,R115,R127,R160,R166
271061100501	RES;10 ,1/16W,5% ,0402,SMT	R113,R231,R86
271061101103	RES;100 ,1/16W,1% ,0402,SMT	R106,R126,R150,R176,R220,R344

Part Number	Description	Location(S)
271061102105	RES;1K ,1/16W,1% ,0402,SMT	R180,R181,R20,R21,R69,R725
271061102303	RES;1K ,1/16W,5% ,0402,SMT	R133,R44,R54,R545,R587,R588,R
271061103501	RES;10K ,1/16W,5% ,0402,SMT	R100,R110,R117,R124,R131,R137
271061104501	RES;100K ,1/16W,5% ,0402,SMT	R109,R112,R25,R26,R338,R347,R
271061105501	RES;1M ,1/16W,5% ,0402,SMT	R136,R29,R310,R360,R636,R746,
271061106501	RES;10M ,1/16W,5% ,0402,SMT	R135
271061118211	RES;11.8K,1/16W,1%,0402,SMT	R737
271061121312	RES;12.1K,1/16W,1% ,0402,SMT	R308
271061133311	RES;13.3K,1/16W,1%,0402,SMT	PR39,PR41
271061135101	RES;1.3M,1/16W,1%,0402,SMT	PR42,R52
271061151102	RES;150 ,1/16W, 1%,0402,SMT	R622,R623,R624,R635,R82
271061152302	RES;15K ,1/16W,5% ,0402,SMT	R726
271061152501	RES;1.5K ,1/16W,5% ,0402,SMT	R103
271061180101	RES;18.2 ,1/16W,1% ,0402,SMT	R714
271061184302	RES;180K ,1/16W, 5%,0402,SMT	R761
271061201101	RES;200 ,1/16W, 1%,0402,SMT	R125,R76
271061202102	RES;2K ,1/16W,1% ,0402,SMT	R70
271061203102	RES;20K ,1/16W,1% ,0402,SMT	R134,R23,R24,R28
271061220501	RES;22 ,1/16W,5% ,0402,SMT	R22,R356,R39,R544,R601,R645,R
271061221313	RES;220 ,1/16W, 5%,0402,SMT	R324,R326,R328,R331
271061222101	RES;2.2K,1/16W,1%,0402,SMT	R138,R157
271061222501	RES;2.2K ,1/16W,5% ,0402,SMT	R10,R105,R15
271061223102	RES;22K,1/16W,1% ,0402,SMT	R371,R372
271061240101	RES;24.9,1/16W,1% ,0402,SMT	R114,R202,R640,R650,R653
271061241101	RES;240,1/16W,1%,0402,SMT	R119

9. Spare Part List-4

Part Number	Description	Location(S)
271061249211	RES;2.49K,1/16W,1% ,0402,SMT	R736
271061270102	RES;27.4 ,1/16W, 1%,0402,SMT	R67,R71,R94
271061272102	RES;2.7K ,1/16W,1% ,0402,SMT	R210,R211,R212,R592,R593
271061330501	RES;33 ,1/16W,5% ,0402,SMT	R519,R520,R521,R524,R528,R529
271061390501	RES;39, 1/16W, 5%,0402,SMT	R18,R19,R81
271061471501	RES;470 ,1/16W,5% ,0402,SMT	R250,R320
271061472501	RES;4.7K ,1/16W,5% ,0402,SMT	R153,R171,R301,R302,R334,R340
271061473501	RES;47K ,1/16W,5% ,0402,SMT	R541,R542,R712
271061474501	RES;470K ,1/16W,5% ,0402,SMT	R60
271061475111	RES;475 ,1/16W,1% ,0402,SMT	R579
271061499012	RES;49.9 ,1/16W,1% ,0402,SMT	R526,R539,R540,R560,R561,R562
271061499212	RES;4.99K,1/16W,1% ,0402,SMT	R120,R229
271061511302	RES;510 ,1/16W,5% ,0402,SMT	R209
271061549011	RES;54.9 ,1/16W,1% ,0402,SMT	R148,R639,R68,R72
271061560501	RES;56 ,1/16W,5% ,0402,SMT	R236,R237,R238,R239,R240,R241
271061562102	RES;5.6K ,1/16W, 1%,0402,SMT	R821
271061562501	RES;5.6K ,1/16W,5% ,0402,SMT	R339
271061681501	RES;680 ,1/16W,5% ,0402,SMT	R167,R615,R93
271061682501	RES;6.8K ,1/16W,5% ,0402,SMT	R357,R358,R807,R808
271061750501	RES;75 ,1/16W,5% ,0402,SMT	R605
271061753101	RES;75,1/16W,1%,0402,SMT	R11,R12,R4,R546,R549,R682,R68
271061822501	RES;8.2K ,1/16W,5% ,0402,SMT	R140,R154,R161,R163,R169,R170
271062120101	RES;12.1,1/10W,1% ,0402,SMT	R534
271071000002	RES;0 ,1/16W,5% ,0603,SMT	L21,L23,L28,L29,L32,L33,L545,L
271071010301	RES;1 ,1/16W,5% ,0603,SMT	PR37

Part Number	Description	Location(S)
271071100101	RES;10 ,1/16W,1% ,0603,SMT	PR17,PR33,PR38,PR509,PR511,P
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR65
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR55
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR31,PR45,PR502,PR504,PR56,P
271071105101	RES;1M ,1/16W,1% ,0603,SMT	PR27,PR28,PR59
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR517,PR78,PR82
271071124311	RES;124K ,1/16W,1% ,0603,SMT	PR49,PR503
271071127211	RES;12.7K,1/16W,1%,0603,SMT	PR58
271071137271	RES;13.7K,1/16W,.1%,0603,SMT	PR50
271071137311	RES;137K ,1/16W,1% ,0603,SMT	PR89,PR96
271071151101	RES;150 ,1/16W,1% ,0603,SMT	R5,R6,R7
271071182214	RES;18.2K,1/16W,1%,0603,SMT	PR87
271071196111	RES;1.96K,1/16W,1% ,0603,SMT	PR16
271071200101	RES;20 ,1/16W,1% ,0603,SMT	R679
271071202102	RES;2K ,1/16W,1% ,0603,SMT	PR5
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR23
271071203701	RES;20K ,1/16W,.1%,0603,SMT	PR52
271071205101	RES;2M ,1/16W,1% ,0603,SMT	PR21
271071221012	RES;221 ,1/16W,1% ,0603,SMT	R107,R149
271071221301	RES;220 ,1/16W,5% ,0603,SMT	R224,R225
271071232111	RES;2.32K,1/16W,1% ,0603,SMT	PR35
271071232211	RES;23.2K,1/16W,1% ,0603,SMT	PR514
271071249111	RES;2.49K,1/16W,1% ,0603,SMT	PR54
271071249311	RES;249K ,1/16W,1% ,0603,SMT	PR1
271071267211	RES;26.7K,1/16W,1% ,0603,SMT	PR88

9. Spare Part List-5

Part Number	Description	Location(S)
271071287311	RES;287K ,1/16W,1% ,0603,SMT	PR51
271071324111	RES;3.24K,1/16W,1% ,0603,SMT	PR81
271071333101	RES;33K ,1/16W,1% ,0603,SMT	PR505
271071362101	RES;3.6K ,1/16W,1% ,0603,SMT	R766
271071374211	RES;37.4K,1/16W,1% ,0603,SMT	PR97
271071374812	RES;37.4 ,1/16W,1% ,0603,SMT	R345
271071412111	RES;4.12K,1/16W,1% ,0603,SMT	PR8
271071432211	RES;43.2K,1/16W,1% ,0603,SMT	PR6
271071442113	RES;44.2 ,1/16W,1% ,0603,SMT	R346
271071471302	RES;470 ,1/16W,5% ,0603,SMT	PR77,PR84
271071472302	RES;4.7K ,1/16W,5% ,0603,SMT	PR70,PR71
271071478101	RES;4.7 ,1/16W,1% ,0603,SMT	PR518,PR98,PR99
271071499011	RES;499 ,1/16W,1% ,0603,SMT	PR60
271071499111	RES;4.99K,1/16W,1% ,0603,SMT	PR24
271071499311	RES;499K ,1/16W,1% ,0603,SMT	PR501,PR57
271071510301	RES;51 ,1/16W,5% ,0603,SMT	R78,R79,R90
271071511111	RES;5.11K,1/16W,1% ,0603,SMT	PR75
271071523111	RES;5.23K,1/16W,1% ,0603,SMT	PR513
271071536101	RES;5.36K,1/16W,1% ,0603,SMT	PR521
271071562201	RES;56.2K,1/16W,1% ,0603,SMT	PR40
271071562831	RES;56.2 ,1/16W,5% ,0603,SMT	R226,R227,R230,R232
271071576311	RES;576K ,1/16W,1% ,0603,SMT	PR36
271071594101	RES;590K ,1/16W,1% ,0603,SMT	PR507
271071619111	RES;6.19K,1/16W,1% ,0603,SMT	PR48
271071634111	RES;6.34K,1/16W,1% ,0603,SMT	R233

Part Number	Description	Location(S)
271071649111	RES;6.49K,1/16W,1% ,0603,SMT	PR86
271071752101	RES;7.5K ,1/16W,1% ,0603,SMT	PR67
271071806211	RES;80.6K,1/16W,1% ,0603,SMT	PR3,PR66
271071806812	RES;80.6 ,1/16W,1% ,0603,SMT	R179,R205
271071976311	RES;976K ,1/16W,1% ,0603,SMT	PR53
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP501
271611220301	RP;22*4 ,8P ,1/16W,5% ,0612,SMT	RP502
271621103302	RP;10K*8 ,10P,1/32W,5% ,1206,SMT	RP3
271621472302	RP;4.7K*8,10P,1/32W,5% ,1206,SMT	RP2
272001105402	CAP;1U ,CR,10V,10%,0805,X5R,SMT	PC30
272001105403	CAP;1U ,10%,10V ,0805,X7R,SMT	PC28,PC551,PC565,PC567
272001106401	CAP;10U ,+-10%,6.3V ,0805,X5R,SMT	PC31
272001106702	CAP;10U,6.3V,+- 20%,0805,X5R,SMT	C116,C144,C145,C146,C148,C151
272001106703	CAP;10U,10V,+80-20%,0805,Y5V,SMT,YAGEO	C141,C173,C177,C201,C206,C37,
272001475701	CAP;4.7U ,CR,10V ,+80-20%,0805,Y5V,SMT	C112,C143,C154,C27,C299,C314,
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y5V	C153,C228,C230,C232,C242,C244
272002475701	CAP;4.7U ,CR,16V ,+80-20%,0805,Y5V,SMT	PC12
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,Y5V	C582
272005104402	CAP;.1U ,50V,+/-10%,0805,X7R,SMT	PC29,PC32,PC558
272005104404	CAP;.1U,CR,50V,10%,0805,SMT	PC4
272011106407	CAP;10U,10V,+/-10%,1206,X5R,SMT,AVX	PC539
272011226401	CAP;22U,6.3V,+-20%,1206,X5R,SMT	C736,PC568,PC569,PC570
272011226701	CAP;22U ,CR,10V,1206,Y5V,+80~20%	C245
272013106502	CAP;10U,25V,+/-20%,1206,X5R,SMT	PC511,PC516,PC517,PC562
272013475402	CAP;4.7U ,25V ,10%,1206,X5R,SMT,PANASONIC	PC508,PC514,PC527,PC534,PC53

9. Spare Part List-6

Part Number	Description	Location(S)
272030102401	CAP;1000P,2KV,10%,1808,X7R,SMT	C215,C336,C337,C338,C339
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5V	PC2,PC3,PC554,PC555,PC556,PC
272071225401	CAP;2.2U ,CR,6.3V ,10%,0603,X5R,SMT	C107,C286,C288,C289,C293,C302
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SMT	PC23
272072104404	CAP;.1U ,16V ,10%,0603,X7R,SMT	PC11
272072683403	CAP;.068U,16V,+-10%,0603,X7R,SMT	PC560
272073223401	CAP;.022U,CR,25V ,10%,0603,X7R,SMT	C101,C103,C92,C93,C95,C97,C99
272073332401	CAP;3300P,CR,25V ,10%,0603,X7R,SMT	PC17
272075101302	CAP;100P ,CR,50V,5%,0603,NPO,SMT	PC19,PC7
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SMT	PC10,PC18,PC25,PC33,PC34,PC5
272075102701	CAP;1000P,50V ,+/-20%,0603,X7R,SMT	PC35,PC36
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,SMT	PC16,PC24,PC38,PC40,PC510,PC
272075103501	CAP;.01U ,50V ,20%,0603,X7R,SMT	PC13,PC27,PC501,PC502,PC505
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,SMT	PC1,PC14,PC15,PC22,PC39,PC50
272075120301	CAP;12P ,CR,50V ,5% ,0603,NPO,SMT	C294,C296
272075221302	CAP;220P ,50V ,5% ,0603,NPO,SMT	PC6
272075222401	CAP;2200P,50V ,10%,0603,X7R,SMT	PC21
272101474702	CAP; .47U ,CR,10V,+80-20% ,0402,Y5V,SMT	C105,C118
272102104401	CAP;.1U ,CR,10V,10%,0402,X5R,SMT	C106,C109,C110,C117,C124,C125
272102105701	CAP;1U ,CR,6.3V ,80-20%,0402,Y5V	C120,C123,C136,C165,C166,C167
272102224701	CAP;.22U ,10V ,+80-20%,0402,Y5V,SM	C119,C590,C751
272105100303	CAP;10P ,CR,50V ,5%,0402,NPO,SMT	C10,C11,C12,C121,C122,C13,C16
272105101402	CAP;100P ,50V ,+ -10%,0402,NPO,SMT	C14,C15,C333,C334,C531
272105102408	CAP;1000P,CR,50V,10%,0402,X7R,SMT	C327,C328
272105103402	CAP;.01U ,CR,25V ,10%,0402,X7R,SMT	C138,C140,C204

Part Number	Description	Location(S)
272105103702	CAP;.01U ,50V,+80-20%,0402,SMT	C281,C534,C583,C600,C601,C602
272105104701	CAP;.1U ,16V,+80-20%,0402,SMT	C100,C102,C104,C108,C111,C113
272105200401	CAP;20P ,50V,+-10%,0402,SMT	C609,C616
272105220402	CAP;22P ,50V ,+ -10%,0402,NPO,SMT	C317,C318,C585,C586
272105222501	CAP;2200P,50V ,+/-20%,0402,X7R,SMT	C335,C574,C575
272105270303	CAP;27P ,50V ,5%,0402,COG,SMT	C661,C662
272105271403	CAP;270P ,50V,+-10%,0402,X7R,SMT	C223,C226
272105392501	CAP;3900P,50V,+/-20%,0402,X7R,SMT	C128,C129,C290,C291
272105470402	CAP;47P ,50V ,+ -10%,0402,NPO,SMT	C156,C157,C158,C159
272105560302	CAP;56PF ,CR,50V,5% ,0402(1005),NPO,0.5A,SMT	C524,C525
272431157507	CAP;150U ,TPC,6.3V,20%,H1.9,7343	C571
272431227528	CAP;220U,2.5V,TPE-MC,20%,POSCAP,H1.8,7343,SM	C587,C598,PC37,PC522,PC523,PC
272431227402	CAP;220U,2V,-35/+10%,H1.9,S,SP-CAP	
272431475001	CAP;470U,2.5V,TPB,7343,SANYO	C593,C595
272602107501	EC;100U,16V,M,6.3*5.5,-55+85'C,SMT	C504,C505,C552
272603276501	EC;27U,23V,+/-20%,F60,H5.7,Polymer,PXA23VC27M	PC513,PC520
272625470401	CP;47P*4 ,8P,50V ,10%,1206,NPO,SMT	CP1
273000111002	CHOKE COIL;120OHM/100MHZ,20%,3216	L51,L523
273000130038	FERRITE CHIP;600OHM/100MHZ,1608,SMT	L12,L13,L14,L15,L17,L18,L19,L2
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,SMT	L10,L11,L2,L3,L4,L5,L544,L55,L
273000150156	FERRIET CHIP;120OHM/100MHZ,2012,6A,MAGIC	PL501,PL502,PL505,PL506,PL50
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,6A	
273000150307	FERRITE BEAD;120 OHM/100MHZ,3A,0805,MAG	L515
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012,TDK	L26,L63,L64,L67,L68
273000150332	FERRIET CHIP;120OHM/100MHZ,2012,5A,MAGIC	L16,L27,L34,L35,L37,L38,L39,L4

9. Spare Part List-7

Part Number	Description	Location(S)
273000150352	CHOKE COIL;QXC24CD121U,120OHM/100MHZ,201	L501,L502,L503,L504
273000500249	CHOKE COIL;2.2UH,30%,Idc=8.5A,H=4mm,SPC-100	PL511,PL514
273000500250	CHOKE COIL;0.68UH,20%,Idc=34A,H=5mm,PCMC13	PL504
273000990021	INDUCTOR;33uH,CDRH124,SUMIDA,SMT	PL507
273000990179	INDUCTOR;3.9UH,30%,SPC08045,H4.5,TMP,SMT	PL512
273000990185	INDUCTOR;3.9UH,30%,CDRH8D43,H4.5,SUMIDA,SMT	
273000990180	INDUCTOR;3.0UH,30%,SPC06703,H2.85,TMP,SMT	PL503
273000990186	INDUCTOR;3.0UH,30%,CDRH6D28,H2.85,SUMIDA,SMT	
273001050210	XSFORMER;10/100/1000BASE TX,NS692403,SMT	U514
274011431449	XTAL;14.318MHZ,32PF,50PPM,8*4.5,2P	X501
274012457406	XTAL;24.576MHZ,16PF,50PPM,8*4.5,2P	X506
274012457426	XTAL;24.576MHZ,16PF,30ppm,8*4.5,2P,eCERA	X504
274012500424	XTAL;25MHZ,20PF,30PPM,8.0*4.5,2P	X505
274012500434	XTAL;25MHZ,30PPM,12PF,8*4.5,2P,F82500049,SM	X1
274013276103	XTAL;32.768KHZ,20PPM,12.5PF,CM200	X503
274018000303	XTAL;8MHZ,30PPM,16PF,8*4.5,2P,SMT,eCERA	X502
281307085001	IC;NC7SZ08P5,2-INPUT & GATE,SC70-5P	U515,U526
282074212503	IC;SN74LVC2G125DCU,VSSOP8	U2
282574008005	IC;74AHC08,QUAD 2-I/P AND,TSSOP,14P	U10
282574014004	IC;74AHC14,HEX INVERTER,TSSOP,14P	U520,U7
282574132001	IC;74AHCT1G32,SINGLE OR GAT,SOT23-5	U502
283467540001	IC;EEPROM,M24C02-WMN6T,2K,SO8,SMT	U12
283467540002	IC;EEPROM,M93C46-WMN6T,64*16 BITS,SO8,SMT	U521
284500655003	IC;ALC655,AUDIO CODEC,LQFP,48P,SMT	U3
284500915001	IC;915GM,Graphics Memory Controller Hub(GMCH),N	U512

Part Number	Description	Location(S)
284504510001	IC;PCI4510GHK,PC CARD,1394A CONTROLLER,BG	U517
284507460002	IC;ADT7460,TEMPERATURE MTR,QSOP,16P,SMT	U507
284508110003	IC;RTL8110SBL,LQFP,128P	U519
284582801073	IC;FW82801FBM,ICH6-M,South Bridge,BGA,609P,Int	U513
284595422001	IC;ICS954226,CTL HUB FOR P4,TSSOP56	U501
286000486001	IC;SC486,DDR MEMORY,PWM CTRL,MLPQ24,SEM	PU511
286100212001	IC;TPA0212,AMPLIFIER,TSSOP,24P,SMT	U5
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU2
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT23	PQ7
286300594001	IC;TL594C,PWM CONTROL,SO,16P	PU3
286300690001	IC;GMT690B,RESET CIRCUIT,2.93V,SOT23	U11
286300961001	IC;G961,1A LOW-DROPOUT,SOT89-5L	U518
286301116001	IC;GS1116Y,0.8A,ADJ,REG,SOT89,SMT	U8
286302211004	IC;TPS2211A,POWER INTERFACE SW,SSOP16	U13
286303107001	IC;AMS3107C,3.3V,1%,VOL REGULATOR,SOT-223	U508
286303734001	IC;LTC3734,PWM CONTROLLER,32-QFN,SMT	PU1
286306227002	IC;ISL6227CA, PWM CONTROLLER SSOP,SMT	PU4
286307805012	IC;78L05,VOLT REGULAT,SOT-89,3P,100MA,SMT	U509
286308800001	IC;AME8800,0.3A,1.5%,LDO,SOT89	U523
286308800014	IC;AME8800,0.3A,1.5V,REG,SOT89	U522
286308800022	IC;AME8800MEFT,0.3A,1.8V,REG,SOT89N,SMT	U14
286309167001	IC;RT9167-47CB,200MA LDO REGULATOR,SOT-25	U504
286369229301	IC;G692L293T,RESET CIRCUIT,2.93V,SOT143,SMT	U511
286388804001	IC;88SA8040,SERIAL ATA BRIDGE,TQFP64	U16
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	D15,PD6

9. Spare Part List-8

Part Number	Description	Location(S)
288100034004	DIODE;SSA34,40V,3A,SMA	PD2,PD503,PD505
288103104001	DIODE;EC31QS04-TE12L,40V,3A,SMT	
288100054002	DIODE;BAT54C,SCHOTTKY DIODE,SOT23	D12,D14,D16,D19,D20,PD5
288100056003	DIODE;BAW56,70V,215mA,SOT-23	D10,D13
288100056017	DIODE;BAW56LT1,70V,215MA,SOT-23,ON	
288100056017	DIODE;BAW56LT1,70V,215MA,SOT-23,ON	PD7
288100099001	DIODE;BAV99,70V,450MA,SOT-23	D1,D2,D5
288100099012	DIODE;BAV99LT1,70V,450MA,SOT-23,ON	
288100099012	DIODE;BAV99LT1,70V,450MA,SOT-23,ON	PD3,PD4
288100140007	DIODE;B140,40V,1A,SMA,DIODES,SMT	PD1
288100014010	DIODE;SS14,40V,1A,SMA,VISHAY	
288100140008	DIODE;SCS140P,40V,1A,SECOS,SMT	PD508
288100541002	DIODE;BAT54ALT1,COM. ANODE,SOT-23	D18
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D11,D17,D31,D502
288100070006	DIODE;BAV70LT1,70V,225MW,SOT-23,ON	
288104148013	DIODE;IN4148W,200MA,500MW,MEL only diodes	D501
288104148001	DIODE;RLS4148,200MA,500MW,MELF,SMT	
288105515001	DIODE;BZV55-C15,ZENER,5%,SOD-80,500mW	PD502
288105524002	DIODE;BZV55-C2V4,ZENER,5%,SOD-80,500MW	PD504
288200114008	TRANS;DDTC114TCA,NPN,SOT-23,DIODES	Q26,Q523,Q524
288200114006	TRANS;DTC114TKA,NPN,SOT23,SMT,PANASONIC(UNR221500L)	
288200144009	TRANS;DDTC144WCA,NPN,SOT-23,SMT	Q510
288200144019	TRANS;DTC144WK,NPN,SOT-23,SMT,PANASONIC(UNR221E00L)	
288200144011	TRANS;DDTC144TCA,NPN,SOT-23,SMT	Q10,Q13,Q15,Q17,Q19,Q21,Q22,(
288200144020	TRANS;DTC144TKA,NPN,SOT-23,SMT,PANASONIC(UNR221000L)	

Part Number	Description	Location(S)
288200301001	TRANS;FDV301N,N-CHANNEL,SOT23	Q513
288202222019	TRANS;MMBT2222ALT1,NPN,TO236AB,ON	PQ10
288202222001	TRANS;MMBT2222AL,NPN,TO236AB	
288202237002	TRANS;MUN2237T1,NPN,SOT-23,SMT,ON	PQ501
288200144019	TRANS;DTC144WK,NPN,SOT-23,SMT,PANASONIC(UNR221E00L)	
288202301006	TRANS;AM2301P,P-MOSFET,SOT-23	Q14,Q16,Q27,Q505,Q508,Q514,Q
288203414001	TRANS;AO3414,N-CHANNEL FET,SOT-23	Q12,Q503
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236AB	Q522
288203904022	TRANS;MMBT3904L,NPN,Tr35NS,TO236AB,ON	PQ2,PQ3
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236AB	
288204406001	TRANS;AO4406,N-MOS,.0165OHM,SO8	PU504,PU506,PU509
288206694002	TRANS;FDS6694,N-MOSFET,SO8,SMT	
288204410010	TRANS;AO4410,N-MOSFET,ID=18A,0.0065OHM,SO	PU501,PU502,PU503,PU510
288207788001	TRANS;FDS7788,18A,30V,5mOHM,SO8	
288204435003	TRANS;FDS4435,P-MOSFET,35mOHM,SO,8P,MRS	Q5,U505,U6
288204407001	TRANS;AO4407,P-MOS,.01OHM,SO8,SMT	
288204419001	TRANS;AO4419,P-MOSFET,20mOHM(VGS=-10V),SO,8P,SMT	
288204914001	TRANS;AO4914,DUAL N-MOSFET,WITH SCHOTTK	PU507,PU508
288221371002	TRANS;MUN2137T1,PNP,SMT,ON	PQ8
288200144023	TRANS;DTA144WK,PNP,SOT23,SMT,PANASONIC(UNR211E00L)	
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SOT-23	Q1,Q11,Q18,Q20,Q25,Q4,Q504,Q
288227002006	TRANS;2N7002LT1,N-CHANNEL FET,ESD	
288227002006	TRANS;2N7002LT1,N-CHANNEL FET,ESD	PQ1,PQ4,PQ5,PQ502,PQ6,PQ9
291000010209	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,SMT,ACES	J510
291000010303	CON;HDR,MA,3P*1,1.25MM,H4.2,ST,SMT,ACES	J511

9. Spare Part List-9

Part Number	Description	Location(S)
291000012031	CON;HDR,MA,10P*2,1MM,H5.4,R/A,SMT,ACES-881	J1
291000020206	CON;HDR,MA,2P*1,1.25MM,H2.57,R/A,SMT,ACES	J509,J513
291000020408	CON;HDR,MA,4P,1.25MM,H3.5MM,R/A,SMT,ACES	J515
291000024426	CON;HDR,FM,22P*2,2MM,R/A,SMT,SUYIN,200062F	J519
291000143007	CON;FPC/FFC,88018-3000,15P*2,.8MM,BD/BD,SMT	J522
291000152603	CON;FPC/FFC,26P,1MM,R/A,KBD,SMT	J2
291000251246	MINIPCI SOCKET;124P,R/A,0.8MM,H=6,SMT,B27-1	J520
291000256843	CON;IC CARD,68P,UP,STANDOFF 0.0 MM ,MPT,29	J5
291000610032	IC SOCKET;32P,PLCC,TIN,W/O PEGS,SMT	U15
291000614793	IC SOCKET;UPGA479M,479P,MOLEX	U506
291000622036	DIMM SOCKET;DDRII REVERSE,200P,0.6MM,H5.2M	J517
291000622037	DIMM SOCKET;DDRII STANDARD,200P,0.6MM,H5	J521
291000913002	CON;SPEED,30P B/B female SMT CON,T02-109-0297	J506,J507
291000920607	CON;STEREO JACK,6P,W9.5,933100000180,SMT,AC	J508,J525
294011200016	LED;GREEN,H0.8,0603,CL-190G,SMT	D22,D24,D26,D27,D28
295000010048	FUSE;0.5A/15V,POLY SWITCH,SMD	F2
295000010102	FUSE;FAST,3A,32V,1206,SMT,CERAMIC	PF502
295000010141	FUSE;FAST,3A,32VDC,1206,SMT,0433003, only littlefuse	
295000010116	FUSE;FAST, 10A, 86VDC, 6125,SMT	PF501
295000010077	FUSE;NANO,10A/32V,R451,SMT	
295000010140	FUSE;FAST,2A,63VDC,1206,SMT,0433002	F1
295000010103	FUSE;FAST,2A,32V,1206,SMT,CERAMIC	
295000010163	FUSE;NORMAL,7A/24VDC,0433007,1206,LITTELFU	PF503
295000010020	FUSE;NORMAL,7A/24VDC,1206,SMT	
295000100004	FUSE;FAST,1A,63V,1206,THIN FILM	F501

Part Number	Description	Location(S)
295000010105	FUSE;1A,NORMAL,1206,SMT	
297040100033	TF041-TH-SW;PUSH BUTTOM,5P,SPST,12VDC,50m	SW1,SW2
331000004009	CON;IEEE1394,MA,4P*1,0.8MM,R/A	J514
331000007056	CON;BATT,C10367-10701,7 PIN,ALLTOP	J504
331040050023	CON;HDR,BTB R/A,0.8MM,S-TECH1507,DIP,50P,AL	J512
331720015084	CON;D,FM,15P/3R,R/A,070915FR015S201ZU,SUYIN,	J501
331840010008	CON;STEREO JACK,10P,W/SPDIF,R/A,GP1FD310TP	J505
331870007007	CON;MINI DIN,7P,R/A,W/GROUND,33007S-07T	J502
342600002081	FINGER;EMI GROUNDING SMD FINGER H=7.0MM,S	TP100,TP503,TP98
342674500002	STAND OFF;AM20-30,GP3	MTG501,MTG502
343685200001	EMI FINGER;3X2MM,H2.5,SME-0025RA,U-TEK	TP5,TP71
481686900002	F/W ASSY;KBC,8066	U510
242600000145	LABEL;10*10,BLANK,COMMON	
284583950002	IC;W83L950D-Ver.C,LPC_KBC,LQFP,80P,SMT	
273000150033	PHASEOUT;FERRITE CHIP,120OHM/100MHZ,25%,	R1,R501
316686900001	PCB;PWA-8066/M BD	R01
242600000433	LABEL;BLANK,11*5MM,COMMON	
242600000232	LABEL;6*6MM,GAL,BLANK,COMMON	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
361200001018	CLEANNER;YC-336,LIQUID,STENCIL/PCB SMT,PRC	
361400003037	SOLDER CREAM;SH-6309,SHENMAO,63/37,PRC	
288204825001	TRANS;AM4825,P-MOS,9.3A,19mOHM,SO8,SMT	PQ503,PQ504,PQ505
273000500115	CHOKE COIL;400uH MIN,120mΩ MAX;TWI	L505,L507

9. Spare Part List-10

Part Number	Description	Location(S)
291000810222	CON;PHONE JACK,2 IN 1,7.0MM,C10037-112A4 -Y	J516
295000010028	FUSE;0.14A/60V,POLY SWITCH,PTC,SMD	F3,F4
331120008011	CON;HDR,SHROUD,MA,8P*1,R/A,88460-08XX,ACE	J6
291000010619	CON;HDR,MA,6P,ACES,87151-0607,SMT	J3
339115000046	MICROPHONE;-62dB+-2dB,D6.0*H2.7,FM-10B1P-07	MIC1
481686900001	F/W ASSY;SYS BIOS,8066	
242600000145	LABEL;10*10,BLANK,COMMON	
283467490002	IC;FLASH,512K*8,FWH,W39V040FAP,PLCC32	
283449004001	IC;FLASH,512*8,FWH/LPC,PM49FL004T-33JC,PLCC32,PMC	
283450040001	IC;FLASH,512*8,FWH,M50FW040K1,PLCC32,ST	
283468180001	IC;FLASH,512K*8,LPC & FWH,SST49LF004B,PLCC32	
283468290003	IC;FLASH,512*8,FWH/LPC,AT49LH004,PLCC32	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242668300028	LABEL;32*7MM,POLYESTER FILM,HOPE	
242600000439	LABEL;25*6,HI-TEMP,COMMON	
370102010502	SPC-SCREW;M2 L5,NIB,K-HD,t0.8,NLK	
370102030301	SPC-SCREW;M2L3,K-HD,1,NIB/NLK	
422677000008	WIRE ASSY;BATT TO MB,FOR LYNX,MOLEX	
346686900006	INSULATOR;DDR,8066	
346686900007	INSULATOR;PCMCI,8066	
343677100001	HEATSINK;NORTHBRIDGE,BANIAS,LYNX	
345686900004	SPONGE;SPEAKER,LEFT,MB,8066	
347207060007	GASKET;2,07,060,007,TennRich	
347207040005	GASKET;2,07,040,005	

Part Number	Description	Location(S)
347205030025	GASKET;2,05,030,025,TennRich	
345686900007	SPONGE;RTC,BATT,8066	
346684000014	INSULATOR;RJ11,BACK,8050M	
331000000314	CON HOLDER;PCMCIA,R-BTN ,MPT,929100000241	J5
346686900021	INSULATOR;MB,8066MP	
347210010010	GASKET;2,10,010,010,TennRich	
347110003015	GASKET;1,10,003,015	
347210003010	GASKET;2,10,003,010,TennRich	
411686920004	PWA;PWA-8066MP,DAUGHTER BD	
411686920005	PWA;PWA-8066MP,DAUGHTER BD,T/U	
411686920006	PWA;PWA-8066MP,DAUGHTER BD,SMT	
271002472301	RES;4.7K ,1/10W,5% ,0805,SMT	PR517,PR518
271035012712	RES;.012,1W,1%,2010,CYNTEC,SMT	PR525
271035012711	RES;.012,1W,1%,2010,LR2010,IRC,SMT	
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR511,PR526
271061000002	RES;0 ,1/16W,0402,SMT	R3
271061102303	RES;1K ,1/16W,5% ,0402,SMT	R1,R4
271061333501	RES;33K ,1/16W,5% ,0402,SMT	R501,R506
271061473501	RES;47K ,1/16W,5% ,0402,SMT	R504,R505
271071000002	RES;0 ,1/16W,5% ,0603,SMT	PR521,PR524,R2
271071100101	RES;10 ,1/16W,1% ,0603,SMT	PR1,PR2
271071103101	RES;10K ,1/16W,1% ,0603,SMT	PR506
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR515,PR516,PR522
271071105301	RES;1M ,1/16W,5% ,0603,SMT	PR512,PR513,PR523
271071107311	RES;107K ,1/16W,1% ,0603,SMT	PR510

9. Spare Part List-11

Part Number	Description	Location(S)
271071196211	RES;19.6K,1/16W,1% ,0603,SMT	PR508
271071202102	RES;2K ,1/16W,1% ,0603,SMT	PR505
271071203101	RES;20K ,1/16W,1% ,0603,SMT	PR504
271071204101	RES;200K ,1/16W,1% ,0603,SMT	PR502,PR503
271071221302	RES;22 ,1/16W,5% ,0603,SMT	R502,R507
271071228301	RES;2.2 ,1/16W,5% ,0603,SMT	PR519,PR520
271071634211	RES;63.4K,1/16W,1% ,0603,SMT	PR509
271072474101	RES;470K ,1/10W,1% ,0603,SMT	PR514
272001105403	CAP;1U ,10%,10V ,0805,X7R,SMT	PC1
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,Y5V	PC503
272005104404	CAP;.1U,CR,50V,10%,0805,SMT	PC518,PC519
272011106404	CAP;10U,6.3V,10%,1206,X7R,SMT	PC517,PC540,PC541,PC546,PC54
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SMT	PC522,PC544,PC545
272075102403	CAP;1000P,CR,50V,10%,0603,X7R,SMT	PC510,PC511,PC515,PC521,PC53
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,SMT	PC2,PC504,PC508,PC516,PC520,
272075152401	CAP;1500P,CR,50V,10%,0603,X7R,SMT	PC513,PC514
272075181301	CAP;180P ,50V ,5% ,0603,NPO,SMT	PC501,PC502
272075470302	CAP;47P ,CR,50V ,5%,0603,NPO,SMT	PC506,PC507
272102105701	CAP;1U ,CR,6.3V ,80-20%,0402,Y5V	C505,C508
272105102501	CAP;1000P,50V ,+/-20%,0402,X7R,SMT	C3,C504,C506,C9
272105103702	CAP;.01U ,50V,+80-20%,0402,SMT	C7
272105104701	CAP;.1U ,16V,+80-20%,0402,SMT	C1,C5,C8
272105471403	CAP;470P ,50V,10%,0402,X7R,SMT	C502,C507,C509
272431157507	CAP;150U ,TPC,6.3V,20%,H1.9,7343	C503,C512,PC542,PC543
272431157512	CAP;150U,6.3V,+/-20%,H2.8,PT,NCC	

Part Number	Description	Location(S)
273000130039	FERRITE CHIP;130OHM/100MHZ,1608,SMT	L10,L12
273000150156	FERRIET CHIP;120OHM/100MHZ,2012,6A,MAGIC	PL501,PL502,PL503
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,6A	
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012,TDK	L2,L6,L7
273000150332	FERRIET CHIP;120OHM/100MHZ,2012,5A,MAGIC	L11,L13,L501,L502,L503
273000610025	FERRITE ARRAY;120OHM/100MHZ,ONLY TDK.	FA1
273000990167	INDUCTOR;10UH,30%,SPC-10039-100	PL504
286104173001	IC;MAX4173F,I-SENSE AMP,SOT23,6P	PU1
286303728002	IC;LTC3728LX,PWM CTRL,LTC,5X5 QFN,SMT	PU501
286309701003	IC;RT9701CB,POWER DISTRI SW,SOT23-5,5P,RICH	U501,U502
288100024002	DIODE;RLZ24D,ZENER,23.63V,5%,SMT	PD501
288100056017	DIODE;BAW56LT1,70V,215MA,SOT-23,ON	PD502
288100056003	DIODE;BAW56,70V,215mA,SOT-23	
288100140007	DIODE;B140,40V,1A,SMA,DIODES,SMT	PD503,PD505
288100014007	DIODE;SS14,40V,1A,SMA	
288100014010	DIODE;SS14,40V,1A,SMA,VISHAY	
288100840001	DIODE;SM840B,40V,8A,STD-202	PD504
288204825001	TRANS;AM4825,P-MOS,9.3A,19mOHM,SO8,SMT	PQ504
288204407001	TRANS;AO4407,P-MOS,.01OHM,SO8,SMT	
288204914001	TRANS;AO4914,DUAL N-MOSFET,WITH SCHOTTK	PU502,PU503
288227002006	TRANS;2N7002LT1,N-CHANNEL FET,ESD	PQ501,PQ502,PQ503,PQ505,PQ5
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SOT-23	
291000021107	CON;HDR,MA,11P*1,1.25MM,SMT,ACECON	J4
295000010008	FUSE;1.1A,POLY SWITCH,1812,SMT	F501
295000010163	FUSE;NORMAL,7A/24VDC,0433007,1206,LITTELFU	PF501

9. Spare Part List-12

Part Number	Description	Location(S)
295000010193	FUSE;FAST,7A/32V,1206,SMT	
297040100034	SW;PUSH BUTTOM,5P,SPST,12V/50MA,H4.3,W/Z G	SW2,SW3,SW4,SW5
331000008033	CON;USB,FM,H15.64,R/A,4P*2,2522A,SUYIN,TETR	J3
316686900002	PCB;PWA-8066/Daughter BD	R01
273000990054	INDUCTOR;10UH,D124C,+/-20%,TOKO,SMT	PL506
291000913003	CON;SPEED,30P B/B male SMT CON,T03-112-0297	J5,J6
272013475402	CAP;4.7U ,25V ,10%,1206,X5R,SMT,PANASONIC	PC526,PC527,PC528,PC530
291000010421	CON;USB,HDR,FM,4P*1,H6.9,R/A,020133MR004S51	J2
331910002006	CON;POWER JACK,2P,20VDC,5A,DIP	J1
297140200006	SW;COVER SWITCH,SPST,30VDC,0.1A,H13.7,4P,SM	SW1
346686900005	INSULATOR;DAUGHTER,BD,8066	
347210010010	GASKET;2,10,010,010,TennRich	
347210040012	GASKET;2,10,040,012,TennRich	
345686900010	SPONGE;DB,USB,8066	
442680900051	TOUCHPAD MODULE;SYNAPTICS,TM42PUM1950	
523468710051	HDD ASSY;60GB,2.5",MHT2060AT,V40+ FW0022,FUJITSUI,8666	
523402379052	HDD DRIVE;60GB,2.5",MHT2060AT,V40+ FW0022,FUJITSUI	
451686900071	HDD ME KIT;8066	
340686900016	SHIELDING ASSY;HDD,8066	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
323768690003	DDR2 SODIMM MODULE;DDR2 533,256MB,NT256T64UH4A0FM-37B,Nanya	
523468690056	DVD COMBO ASSY; UJ-DA760,PANASONIC,8066	
523410484014	DVD COMBO DRIVE; UJ-DA760,8X24X24X24X, PANASONIC	
451686900061	ODD ME KIT;8066	
342672200010	BRACKET;CD-ROM,8500	

Part Number	Description	Location(S)
370102010201	SPC-SCREW;M2L2,NIW,K-HD,t=0.8,NLK	
340683400010	BEZEL ASSY;COMBO,MKE,730,8050F	
373101713502	T-SCREW;B.M1.7L3.5,HD04t0.25,0,BCT	
441686900011	BATT ASSY;11.1V,4.7AH,3S2P,Li,CGR18650D,PAN,8066MP,MSL POWE	
441686900009	BATT ASSY;8066MP/11.1V,4800mAH,PANASONIC,3S2P,PWR	
222503220001	PE BUBBLE BAG;BATTERY,GRAMPUS	
225600000054	TAPE;INSULATING,POLYESTER FILM,17.5MM,130'C,PRC	
225600000061	TAPE;ADHENSIVE,DOUBLE-FACE,W20,UL,PRC	
226600030332	SPONGE;320*290*10,CAIMAN,PWR	
242669600005	LABEL;LOT NUMBER,RACE	
242683700006	LABEL;48*6mm,EMPTY,WHITE,MIO 136 BATT,PWR	
242686900004	LABEL;BATT,11.1V/4.7AH,LI,PANASONIC,8066MP	
333025000004	SHRINK TUBE;300V,125,I.D=2.5,T=0.15,L=7,BLACK;PWR	
333025000005	SHRINK TUBE;300V,125,I.D=2.5,T=0.15,L=13,BLACK;PWR	
338536010064	BATTERY;LI,3.6V/2.35AH,CGR18650D,PANASONIC,PWR	
342502900001	CONTACT PLATE;W4L27T0.15,7068	
342503200004	CONTACT PLATE;W4L63T0.15,1/4,T TAPE,7521/GRAMPUS	
342683700006	CONTACT PLATE;W5L63T0.13mm,GE BATT,PWR	
342686900010	CONTACT PLATE;T=0.13mm,L=85mm,PWR	
344686900001	COVER;BATTERY,8066	
344686900002	HOUSING;BATTERY,8066	
346502800004	INSULATOR;BATT ASSY,BATT+,BATT-,7368	
346503200202	INSULATOR;BATT ASSY,ONE ROUND,BLAC,WEASEL	
346681800004	INSULATOR;BATT,ASSY,L129W15T0.25MM,8677C,PWR	
346684400004	INSULATOR;FIBER,UL94V-0,2CELL,D=18mm,T=0.25mm,ADHESIVE W204	

9. Spare Part List-13

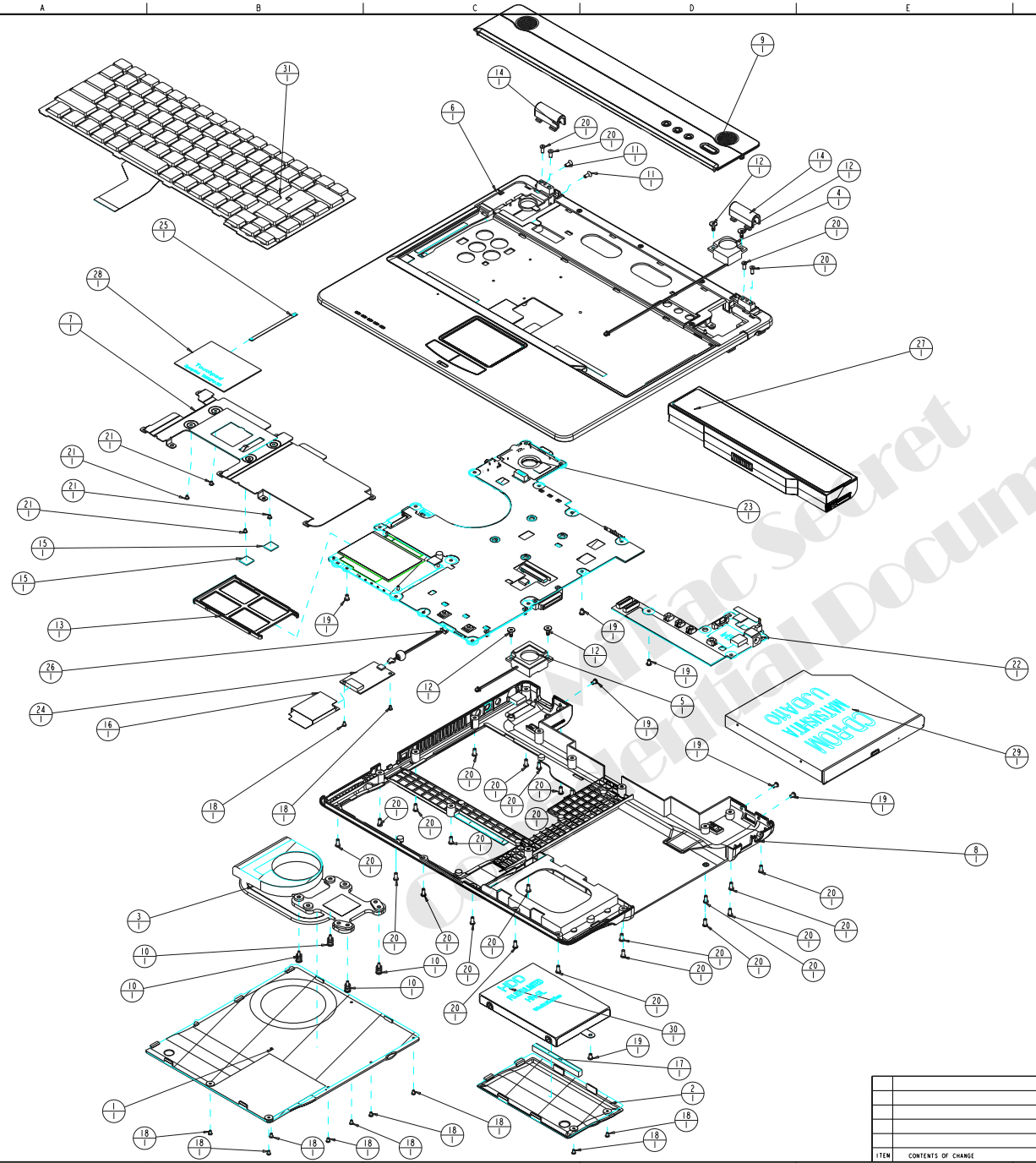
Part Number	Description	Location(S)
346686900012	INSULATOR;FIBRE,T=1.2mm,L=25mm,W=7.5mm,PWR	
346686900015	INSULATOR;FIBER,T=0.25mm,107*12,PCB,PWR	
361400003005	ADHESIVE;HEAT,TRANSFER,HTA-48(W)	
361400003030	ADHESIVE;ABS+PC PACK,G485,CEMIDAIN	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
624200010140	LABEL;5*20,BLANK,COMMON	
411686900022	PWA;PWA-8066MP/BATT PANASONIC 3S2P,BOARD,PWR	
310111103027	THERMISTOR;10K,1%,RA,DISK,103AT-4,only 爲勤	RT1
331000007025	CONNECTOR;7 PIN,DIP,ALLTOP,C10345-10701	CON1
332110020195	WIRE;#20,UL1007,125MM,BLACK,PWR	CN5
332110026133	WIRE;#26,UL1007,93MM,YELLOW,YIYI,PRC,PWR	CN2
332110026135	WIRE;#26,UL1007,40MM,ORANGE,PRC,PWR	CN3
333050000117	SHRINK TUBE;UL,600V,105'C,ID2.5*7MM,8175	
335152000026	CFM-BAT;FUSE,THERMAL,NEC,SF91E	
335152000085	FUSE; 128 DC-7A/50V 139℃only UCHIHASHI（內橋	F2
335152000097	FUSE;LR4-73X,POLY SWITCH,PWR	
361400003003	JET-MELT ADHESIVES;3478-Q,5/8in*8in,PRC	
365350000003	SOLDER WIRE;0.8MM,SN43/PB43/BI14,N/C,TELECORE,PRC	
411686900023	PWA;PWA-8066MP/BATT PANASONIC 3S2P,GAUGE BD,SMT,PWR	
271045059101	RES;0.050,1W, 1%,2512,SMT ,only Cyntec	R24,R24A,R24C
271045507103	RES;0.050,1W, 1%,2512,SMT, only KOA;PWR	
271046019101	RES;0.010,1.5W, 1%,2512,SMT;PWR,only Cyntec	R6
271044100101	RES;0.010,1.5W, 1%,2512,SMT;PWR	
271071000002	RES;0 ,1/16W,5% ,0603,SMT	C16,R31
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R11,R12,R14,R15,R16,R20,R21

Part Number	Description	Location(S)
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R5,R7,R8
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R18,R22,R23,R9
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R10,R3
271071201301	RES;200 ,1/16W,5% ,0603,SMT	R1A,R1B
271071204101	RES;200K ,1/16W,1% ,0603,SMT	R17B
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R1
271071331301	RES;330 ,1/16W,5% ,0603,SMT	C14
271071499311	RES;499K ,1/16W,1% ,0603,SMT	R17A
272005104705	CAP ;1U CR 50V +80-20% 0805 Y5V SMT only TDK	C14A,C14B,C4A,C4B
272075101404	CAP; 0.001U CR 50V 10% 0603 X7R SMT only TDK	C13
272075103408	CAP ;0.1U CR 50V 10% 0603 X7R SMT only TDK	C10,C11,C12,C15,C3,C5,C6,C7,C8
272075223702	CAP; 0.22U CR 50V +80-20% 0603 Y5V SMT only TI	C1,C2,C20A,C24,C25
272075471409	CAP; 0.0047U CR 50V 10% 0603 X7R SMT only TDK	C4
283467540001	IC;EEPROM,M24C02-WMN6T,2K,SO8,SMT	IC2
283467530001	IC;EEPROM,S24CC02A,2K,SO8,SMT,ONLY SEIKO;PWR	
286002040001	IC;BQ2040,GAS GAUGE,SO,16P,SMT	IC1
286300812002	IC;S-812C,DECECTOR,SOT-89,PRC	IC3
286301414001	IC;MM1414,PROTECTION,TSOP-20A,PRC	IC4
288100280001	DIODE; DII S1G ,280V1A,SMA, SMT,PWR	D1
288111544001	DIODE; 1SR-154-400 400V 1.0A SMT	
288105256001	DIODE;BZT52C5V6S,ZENER,5.2-6.0V,200mW,SOD-3	ZD3,ZD4
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SMT	
288110355001	DIODE;1SS355,80V,100mA,SOD-23,SMT	D2
288104148024	DIODE;DII 1N4448HWS,57V250mA,SOD-323,SMT,PWR	
288200144037	TRANS;DII DDTA144EKA,40V100mA ,PNP,SMT,PW	Q1

9. Spare Part List-14

Part Number	Description	Location(S)
288200144008	TRANS;DTA144EKA,PNP,SMT	
288200717001	DIODE;RB717F,SCHOTTKY,40V,SOT323,SMT	D3
288204409001	TRANS;AO4409,P-MOSFET,SO-8P,MSL,PWR	Q3,Q5
316687600003	PCB;PWA-8965-8066/BATTERY BD,PWR	R0A
461686900001	PACKING KIT;NORMAL,8066	
221686920001	CARTON;NON-BRAND,8066	
222670820003	PE BAG;L560*W345,7521N	
222682800001	PROTECTION PAPER;LCD/KB,BEN Q,8089P	
224682800001	PALLET;COMPLEX,1200*1000*126,8089P	
227686900002	END CAP;L/R,NORMAL,8066	
242600000157	LABEL;BAR CODE,125*65,COMMON	
221682850003	CARD BOARD;TOP/BTM,PALLET,BEN Q,8089P	
221682850007	CARD BOARD;FRAME,PALLET,BEN Q,8089P	
221686950001	CARD BOARD;PARTITION,PALLET,8066	
451686900001	LABEL KIT;N-B,8066	
242670800113	BFM-WORLD MARK;WINXP,7521N	
242679900005	LABEL;BAR CODE,(25*10MM)*12pcs,8640C	
242686900002	LABEL;N-B,RATING,8066	
541668690001	AK;N-B,8066	
221682840001	AK BOX;BEN Q,8089P	
222672730001	PE BUBBLE BAG;200*240mm,AMM-9019	
221682850006	PARTITION;BEN Q,AK BOX,8089P	
222671330003	PE BAG;LCD BRACKET,STINGRAY	
222682800002	PE BAG;302*208MM,BEN Q,8089P	
242669900009	LABEL;BLANK,60*80MM,7170	

Part Number	Description	Location(S)
332810000033	PWR CORD;125V/7A,2P,BLACK,AMERICA	
531068540011	KBD;88,UI,K011718M5,JME,BLACK,8011	
442681400053	AC ADPT ASSY;19V,3.42A,DELTA ADP-65DB AV	
		P/N:526268692001



ITEM	PART NO	DESCRIPTION	Q'TY	TYPE	REMARK
1	340686900002	COVER ASSY,CUP,8066	1	ASSEMBLY	
2	340686900003	COVER ASSY,HDD,8066	1	ASSEMBLY	
3	340686900006	HEATSINK ASSY;CPU,8066	1	ASSEMBLY	
4	340686900010	SPEAKER ASSY;R,8066	1	ASSEMBLY	
5	340686900011	SPEAKER ASSY;L,8066	1	ASSEMBLY	
6	340686900018	COVER ASSY;8066MP	1	ASSEMBLY	
7	340686900019	SHIELDING ASSY;COVER,8066MP	1	ASSEMBLY	
8	340686900020	HOUSING ASSY,8066MP	1	ASSEMBLY	
9	340686900021	COVER ASSY;KB,8066MP	1	ASSEMBLY	
10	341677000002	SPRING-SCREW-HEATSINK-LYNX	4	PART	
11	341680900001	SPC SCREW;#4-1/4,8050	2	PART	
12	342686900019	T-SCREW;M26L6.5,8066	4	PART	
13	344684000040	DUMMY CARD;PCMCIA,8050M	1	PART	
14	344686900006	COVER;HINGE,8066	2	PART	
15	345686300002	SPONGE;HDD,8050FX	2	PART	
16	346670500014	INSULATOR;MDC,TETRA	1	PART	
17	347205060060	GASKET;2.05,060,060	1	PART	
18	370102030301	SPC-SCREW; M2L3,K-HEAD,I,NIB,NLK	11	PART	
19	370102610401	SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N	7	PART	
20	370102610603	SPC-SCREW; M2.6L6 K-HEAD,NIB/NLK	26	PART	
21	371102010252	SCREW;M2L2.5,K-HEAD(+),NIB/NLK	4	PART	
22	411686900004	DB ASSY;8066	1	ASSEMBLY	
23	411686920001	MB ASSY;8066MP	1	ASSEMBLY	
24	412671800001	PCB ASSY;FAXMODEM,56K,MDC,GP2	1	PART	
25	422686900001	CABLE FFC;TP,8066	1	PART	
26	422686900007	WIRE ASSY;MODEM,8066MP	1	ASSEMBLY	
27	441686900002	BATT ASSY-8066	1	ASSEMBLY	
28	442680900051	TOUCH PAD;SYNATICS,TM42P-313	1	PART	
29	451680900038	COMBO MEKIT;QSI,SBW242,8050	1	ASSEMBLY	
30	451686900071	HDD;MEKIT,8066	1	ASSEMBLY	
31	531020237661	KBD;89,US,K011718MI,LYNX	1	PART	

ITEM	CONTENTS OF CHANGE	BVS	CHK	APV	M/D/Y
					/ /
					/ /
					/ /
					/ /
					/ /

TOL: RANGE	Plo	Met	Tes	Por	Cab	Pac	Gas	PCB
0-6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6-30	0.1	0.1	.15	.25	1	1	0.5	0.1
30-80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80-180	.15	.15	.25	0.3	2	2	1	.15
180-315	.15	0.2	0.3	0.4	2.5	2	1	.15
315-800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	17-Feb-05	MATERIAL	SEE NOTES	TREATMENT	
UNIT	MM	SCALE	0.50	DRAWING NAME	HOUSING KIT;8666MP
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	MF 451686920051 R00

REMARK

MiTAC Technology Corp.

model name:8666MP-STRU

file name:STRU-8066MP-EXP

SHEET NO. 1 of 1

Reference Material

❖ Intel Dothan Pentium M Processor	Intel.INC
❖ Intel 915GM North Bridge	Intel.INC
❖ Intel ICH6-M South Bridge	Intel.INC
❖ Winbond W83L950D Keyboard BIOS	Winbond.INC
❖ Clock Generator ICS954226	ICS.INC
❖ System Explode View	Technology.Corp./MiTAC
❖ 8066MP Hardware Specification	Technology.Corp./MiTAC

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